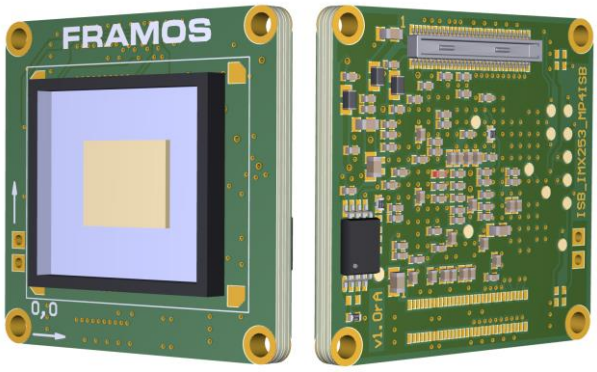
FSM-IMX264 Datasheet

Sony IMX264LLR / IMX264LQR Sensor Module

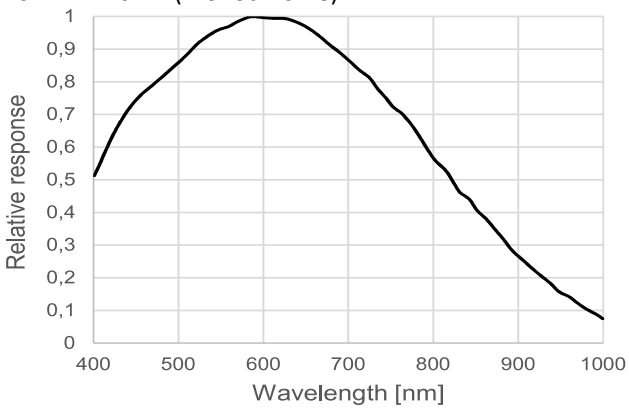
FRAMOS Sensor Module



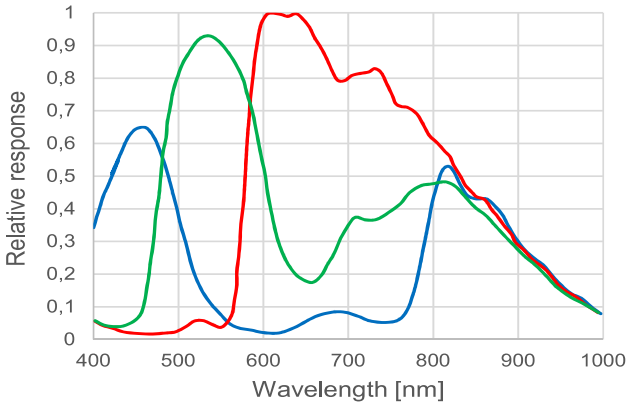
Key Benefits & Features:

- 5.1 Mpx Sony CMOS Global Shutter sensor module, ready to embed!
- All FSMs are part of a rapid prototyping ecosystem, consisting of:
  - ✓ Adapters to various processing boards
  - ✓ Design sources for deep embedding
  - ✓ Various accessories and design in services

FSM-IMX264M (Monochrome):



FSM-IMX264C (Color):



Specification	
Model Name	**FSM-IMX264M / FSM-IMX264C** (V1A)

Image Sensor	
Vendor / Name	Sony IMX264LLR / IMX264LQR
Shutter Type	CMOS Global Shutter
Chromaticity	Color / Mono
Optical Format	2/3“
Pixel Size	3.45 x 3.45 µm
Max. Resolution	5.1 Mpx / 2464 x 2056 px
Framerate (max.)	35.7 FPS (4-Lane)
Bit Depth(s)	12 bit

Interface	
Data Interface	SubLVDS (4 Lane)
Communication Interface	I²C (4-wire serial)
Drive Frequency(s)	37.125 / 54 / 74.25 MHz
Input Voltages	1.2V, 1.8V, 3.3V
Interface Connector	Hirose DF40C-60DP-0.4V(51)
EEPROM (Sensor ID)	Yes

Mechanical	
Dimensions (HxWxD)	28 mm x 28 mm

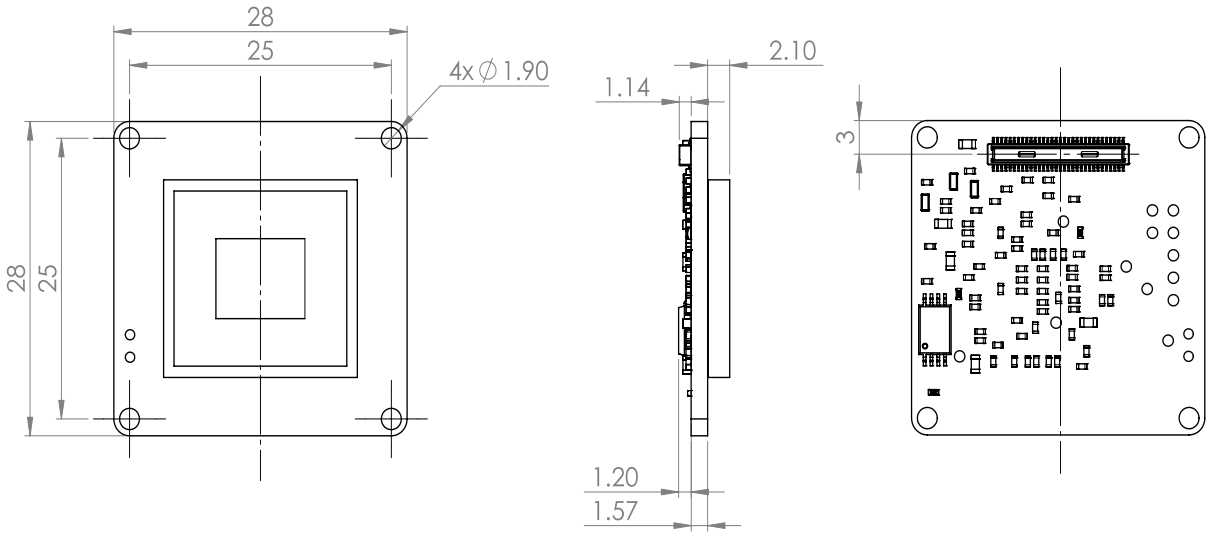
Environmental	
Operating Temperature	-30°C to +75°C (function) -10°C to +60°C (performance)
Storage Temperature	-40°C to +85°C
Ambient Humidity	20% to 95% RH, non condensing

Software Support (requires FSA with MIPI CSI-2 conversion)	
Driver	V4L2 Based Device Driver
Supported Platform(s)	NVIDIA Jetson Family: AGX Xavier, TX2
Software Version(s)	NVIDIA JP4.4 / L4T32.4.3

Suggested Accessories & Adapters	
Compatible FSA	
Recommended Devkit(s)	FSM-IMX485x/TXA_Devkit (TX2, AGX)
Lens Mounts	C/CS-Mount option

A matrix with compatible *Sensor Adapters (FSA)* and *Processor Board Adapters (FPA)* for various setups can be found at the end of this document.

Mechanical Drawing



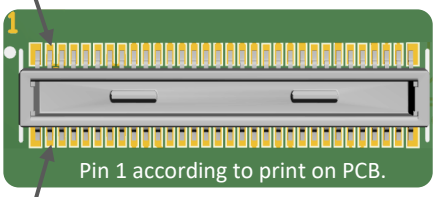
Sensor image optical center is in mechanical board center.

Connector Pinout

Type: Hirose DF40C-60DP-0.4V(51)

Mating Type: Hirose DF40HC(4.0)-60DS-0.4V(51)

Name	NC	NC	3V3	3V3	1V8	GND	GND	SDA	SDO	TOUT0	TOUT1	TOUT2	NC	NC	NC	GND	RST	MCLK	GND	D_DATA_6_P	D_DATA_6_N	GND	D_DATA_4_P	D_DATA_4_N	GND	D_DATA_2_P	D_DATA_2_N	GND	D_DATA_0_P	D_DATA_0_N
Pin	1	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31	33	35	37	39	41	43	45	47	49	51	53	55	57	59



Pin	2	4	6	8	10	12	14	16	18	20	22	24	26	28	30	32	34	36	38	40	42	44	46	48	50	52	54	56	58	60
Name	1V8_EEPROM	1V8_EEPROM	1V2	1V2	NC	GND	GND	SCL	XCE	SLAMODE	XMASTER	NC	XTRIG	XHS	XVS	GND	D_DATA_7_P	D_DATA_7_N	GND	D_DATA_5_P	D_DATA_5_N	GND	D_DATA_3_P	D_DATA_3_N	GND	D_DATA_1_P	D_DATA_1_N	GND	D_CLK_0_P	D_CLK_0_N

Signals are routed directly from image sensor to connector. Details on specific signals are described in the respective image sensor datasheet.

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Table of Contents

Full Datasheet

Certification and Standards

The equipment described in this document is designed for evaluation and laboratory use, as well as for the integration into electronic devices. The customer is responsible to take all necessary precautions to fulfill regulations and laws of end-customer and target market.

Technical Support

The technical equipment described in this document, be it hardware or software, is delivered as it is and does not include any obligations to the FRAMOS GmbH to provide technical customer support. Technical support is granted on project basis arbitrary by the FRAMOS GmbH.

ATTENTION
Electrostatic sensitive devices!
Observe precautions for handling!

Handling ESD Sensitive Components

The electronic components like Printed Circuit Boards (PCB) described in this document are sensitive to Electrostatic Discharge (ESD) and need to be handled with high care in static controlled environments. It is strongly recommended to follow the general handling practices for ESD sensitive parts, that include, but are not limited to, the following points:

- Treat all PCBs and components as ESD sensitive.
- Assume that you will damage the PCB or component if you are not ESD conscious
- Handling areas must be equipped with a grounded table, floor mats and wrist strap
- A relative humidity level must be maintained between 20% and 80% non-condensing
- PCBs should not be removed from their protective package, except in a static controlled location
- PCBs must be handled only after personnel have grounded themselves via wrist straps and mats
- PCBs or components should never come in contact with clothing
- Try to handle all PCBs only by their edges, preventing contact with any components.

FRAMOS is not responsible for any damages caused by ESD on customer side.

1 FRAMOS Sensor Module Ecosystem

The FSM Ecosystem consists of FRAMOS Sensor Modules, Adapters, Software and Sources, and provides one coherent solution supporting the whole process of integrating image sensors into embedded vision products.

During the evaluation and proof-of-concept phase, off-the-shelf sensor modules with a versatile adapter framework allow the connection of latest image sensor technology to open processing platforms, like the NVIDIA Jetson Family or the 96boards.org standard. Reference drivers and sample applications deliver images immediately after installation, supporting V4L2 and an optional derivate API providing comfortable integration. Within the development phase, electrical design references and driver sources guide with a solid and proven baseline to quickly port into individual system designs and extend scope, while decreasing risk and efforts.

To simplify and relieve the whole supply chain, all FRAMOS Sensor Modules and adapters are optimized and ready for delivery in volume and customization with pre-configured lens holder, lens and further accessories.

Off-the-Shelf Hardware

- FRAMOS Sensor Modules (FSM) from stock, ready for evaluation and optimized for initial mass production.
- Versatile adapter framework, allowing flexible testing of different modules, on different processing boards:
  - FRAMOS Sensor Adapter (FSA): Everything the specific sensor needs for operation
  - FRAMOS Processor Adapter (FPA): Connect up to four FSM + FSA to a specific processor board
- From lenses, mechanics and cables, all needed imaging accessories from one hand

Ready to go Software Package

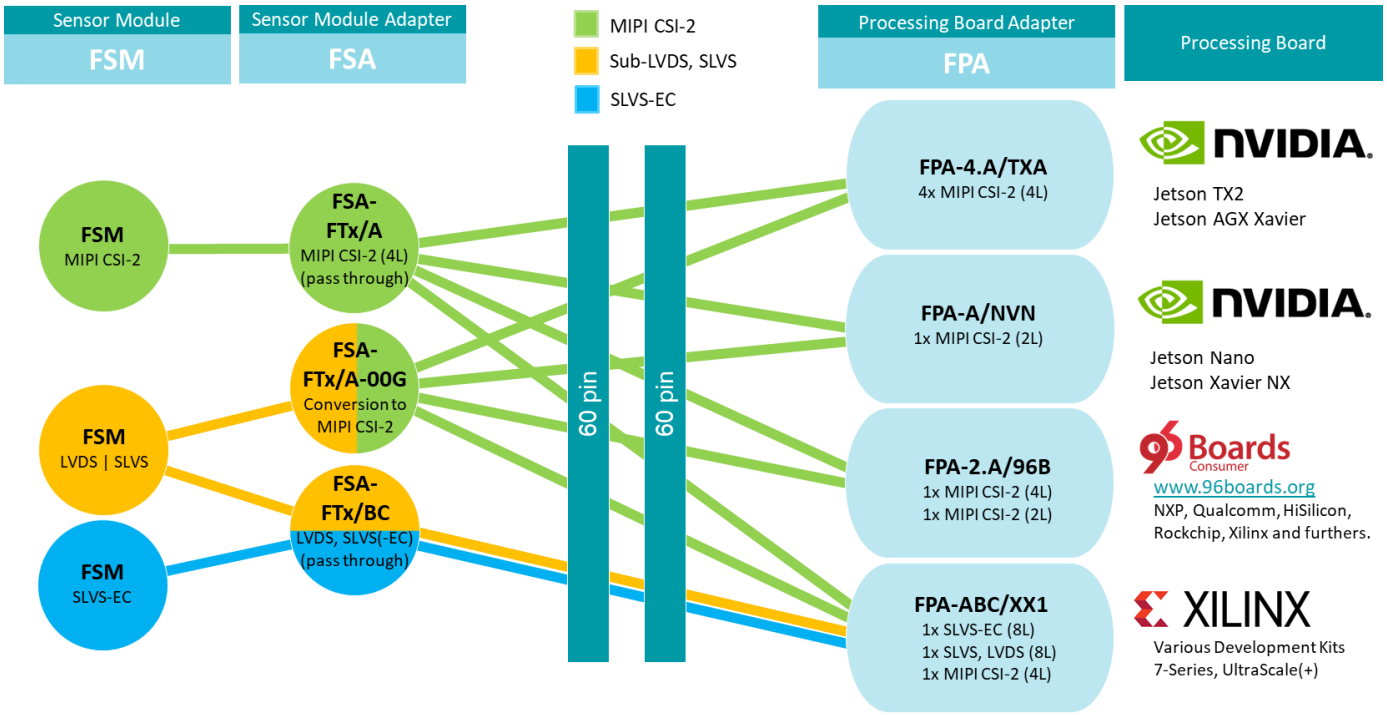
- Drivers with basic sensor integration:
  - Platform specific device drivers
  - V4L2 subdevice drivers for specific image sensors (low-level C API)
- Streamlined V4L2 library (LibSV) with comfortable and generic C/C++ API
- Example applications demonstrating initialization, main configuration and image stream processing

Further to the off-the-shelf hard- and software, the Ecosystem supports you on project basis with:

- Driver sources allowing the focus on application specific scope and sensor features
- Electrical references for FSA and FPA, supporting quick and optimized embedding of FSMs
- Engineering services via FRAMOS and its partners, allowing you to focus on your product's unique value

1.1 Ecosystem Overview

The figure below shows a map of compatibility with all components inside the Ecosystem. Every element (or hardware) and connection displayed in **Green** operates with native MIPI CSI-2 (D-PHY) data.



Every component and connection displayed in **Orange** or **Blue** operates with proprietary (Sub-LVDS, SLVS) or standardized (SLVS-EC) LVDS data, that requires further attention to the physical processing of the image data by either data conversion or specific FPGA IP. Users of MIPI CSI-2 based processing systems are supported by FSM specific data conversion located on dedicated FRAMOS Sensor Adapters (FSAs).

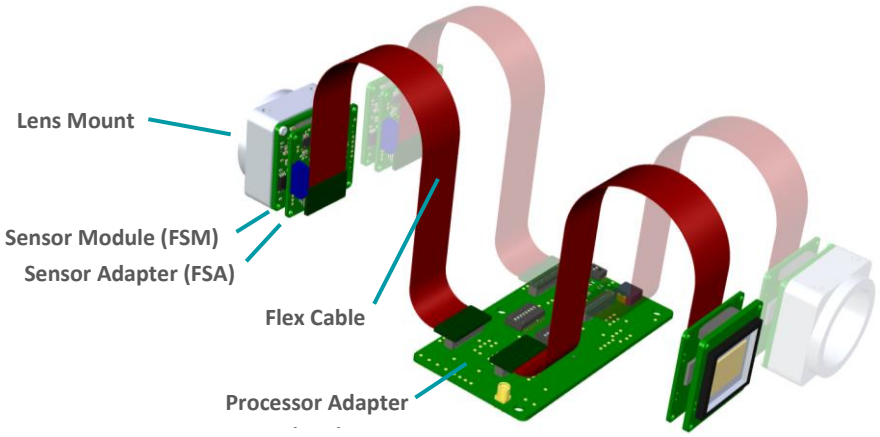


Figure 1: Assembly of a typical Sensor Module Development Kit

Specification and compatibility of all individual components are listed in the appropriate chapter of the full datasheet. Access to software and drivers is only granted with the purchase of the appropriate development kit. Electrical design sources, support and services are provided on individual basis, they are not part of the development kit or component purchase.

1.2 Materials and Services

Below you can find a list of materials and services as part of the FRAMOS Sensor Module Ecosystem.

Hardware

- FRAMOS Sensor Module Development Kits
- Individual Parts:
    - FRAMOS Sensor Modules
    - FRAMOS Sensor Adapters
    - FRAMOS Processor Adapters
    - FRAMOS Module Accessories (Cables, Mounts)

Software (part of the Development Kit)

- Software Package for NVIDIA Jetson AGX Xavier, Nano, TX2 and Xavier NX
- Software Package for DragonBoard 410c (96Boards)
- Xilinx FPGA reference implementation for SLVS-EC (Sony IMX421, IMX530)

Design Sources (on Project Basis)

- Software Driver Sources
- Electrical References for FSA, FPA (Schematics)

Design Services

- Off-the-shelf hardware customization including size, shape, connector and extended functionality
- Software customization and extension
    - Additional processor board support
    - Further sensor features and image (pre-)processing
- Integration of additional sensors
- Optimization for volume production
- Lens assembly and alignment
- System / solution development
- Production and integration

2 Start-Up Instructions

The following chapter describes the hardware assembly procedure by reference to a generalized example. The actual setup depends much on the actually used components and might differ from the description. However, the main steps, rules and cautions apply to every system.

2.1 Hardware Assembly

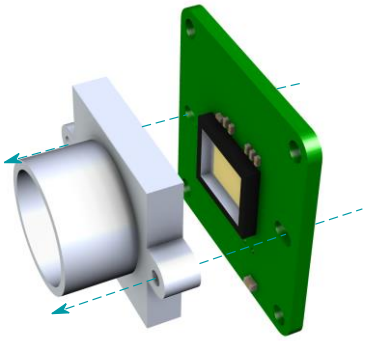
All Development Kits come pre-assembled. It is only required to connect the FSM, FSA and Flex Cable assembly to the FPA and attach it to the appropriate Processor Board.

Required Materials
FRAMOS Sensor Module Development Kit or individual components:

- FSM-xxxxxx
- FSA-FTxx/A
- FPA-xxxxxx
- FMA-FC-150/60-xxxx
- M12 lens mount (optional)

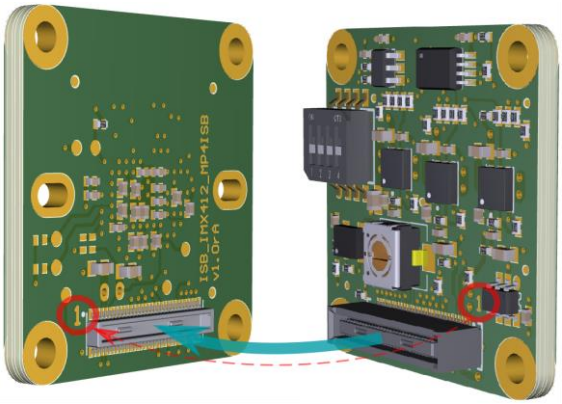
Note: Due to manual alignment requirements for back focal distance and position, C/CS-mounts are regularly shipped already mounted to the FSM.

1. Add M12 lens mount (optional)
Prior to assembling the FSM to the FSA, screw an optional M12 lens mount to the FSM.



Fitting screws are provided with the lens mount. If assembling a 3rd-party mount, please check the hole diameters for the specific module in its technical drawings to select fitting screws.

2. Connect FSM and FSA
Connect the FSM to the FSA, by pressing the two 60 pin connectors together. Watch carefully for the correct connector orientation and the match of both "Pin1".



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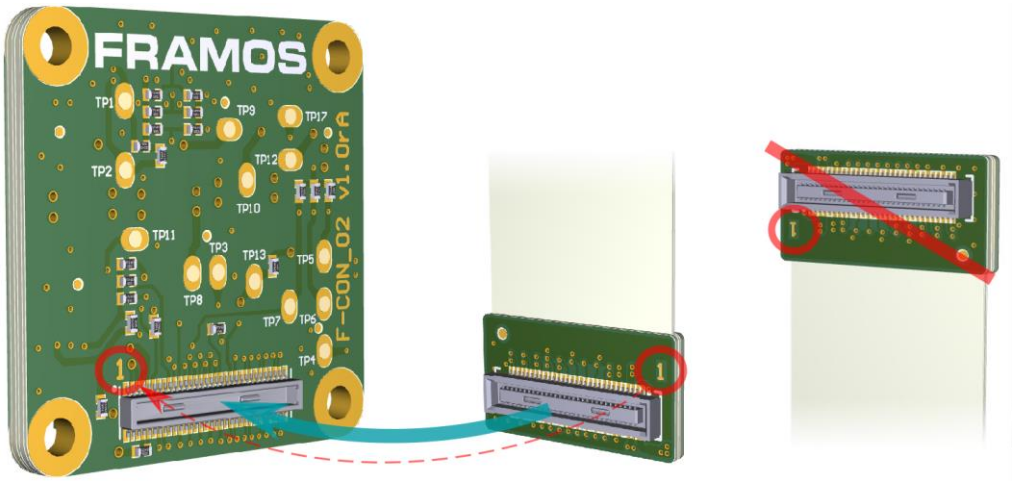
Fix the mechanical connection by using the provided screws with distance holders and nuts between both boards. In case of an C/CS-mount, screw the board stack into the lens mount mechanics instead of using the nuts.

3. Add Flex Cable

Connect the FSM, FSA stack via the connector on the rear side of the FSA to the appropriate side of the FMA-FC-150/60 flex cable.

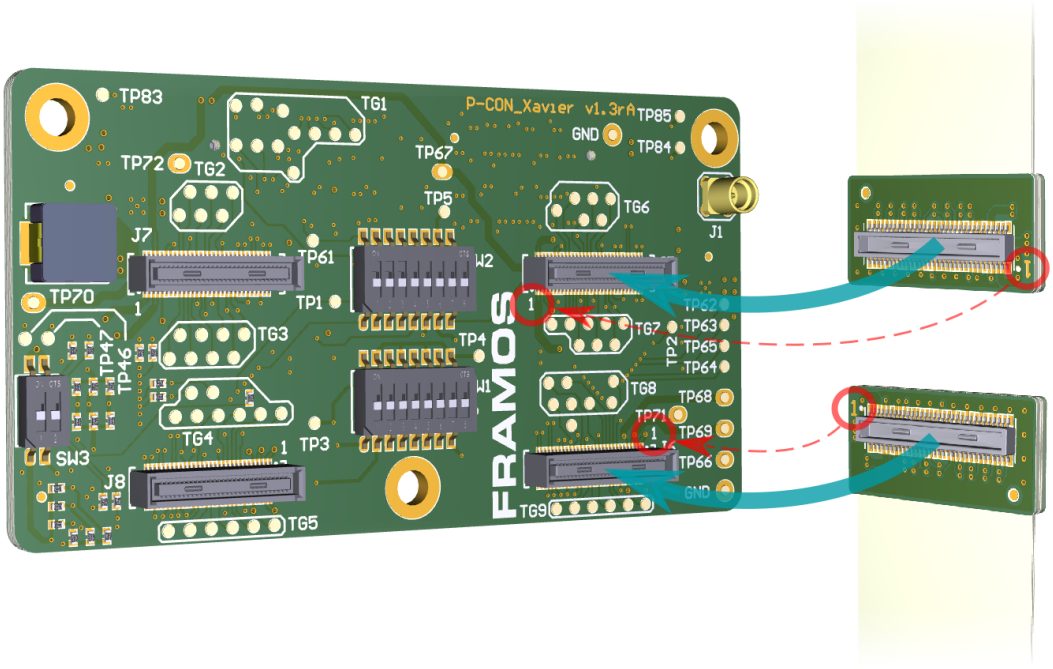


Skip this step, in case you are going to connect a piggy-back FPA like the FPA-A/NVN.

Caution: Direct connection of FSM to FPA (without FSA) or wrong cable orientation will lead to permanent damage of FSM, Adapters or the Processor Board!

4. Connect to FPA

Connect the other side of the flex cable to a sensor connector on the FPA. According to the available sensor interface count, multiple FSM+FSA assemblies can be connected.



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With processor boards like the NVIDIA Jetson TX2 Development Kit, the FPA provides access to only two MIPI CSI-2 lanes on FSM3 (J7) and FSM4 (J8). This might lead to restrictions in combination with some FSMs. For compatibility, please review the connector description of the specific FPA.

Caution: Direct connection of FSM to FPA (without FSA) or wrong cable orientation will lead to permanent damage of FSM, Adapters or the Processor Board!

5. Finalize Assembly
Remove the power supply of the processor board and connect the complete assembly to the processor board. Follow the guidelines of the processor board manufacturer for the appropriate camera connector.

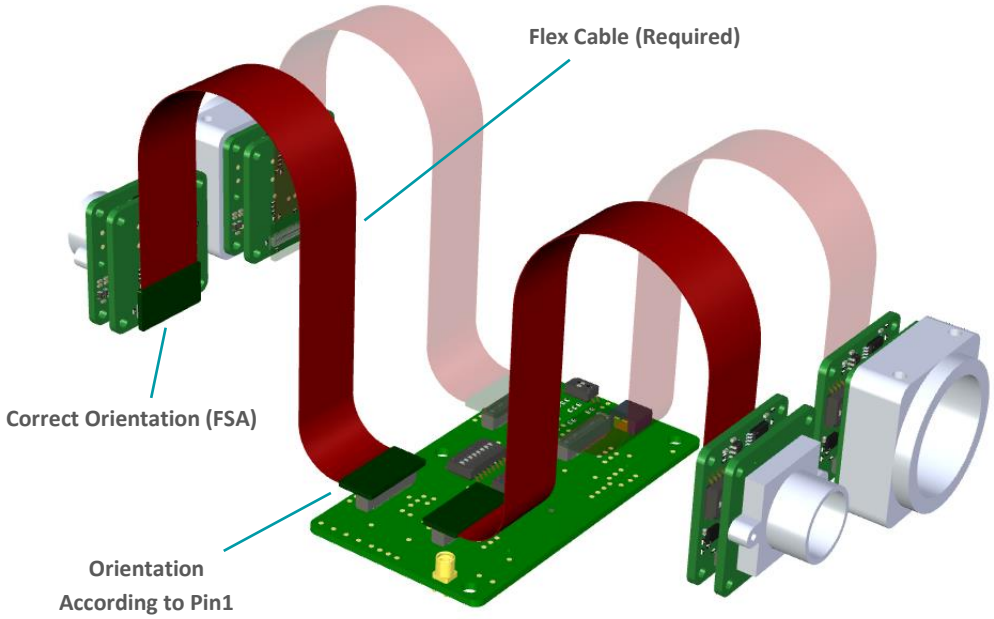


Figure 2: Correct orientation of Flex Cable in an example Multi-Sensor Setup (NVIDIA Jetson)

Power up the processing board and start the software setup.

2.2 Software Setup

For instructions on the setup of the target processor board and driver installation procedure, please refer to the "User Guide" included in the appropriate installation package.

The link to the software download section is included in the Development Kit.

3 FRAMOS Sensor Modules (FSM)

The FRAMOS Sensor Modules are printed circuit boards, interfacing various types of image sensors with standardized connectivity like connector type, pinout, mechanical format and compatible accessories. The target is to provide various sensor boards that can be used 'off the shelf' to connect a variety of image sensors to a host system. Starting from evaluation and proof-of-concept, but also in mass production where adjustments to actual needs are easily possible.

The following chapter provides information on the generic attributes as well as the individual modules, in addition to the individual FSM datasheets.

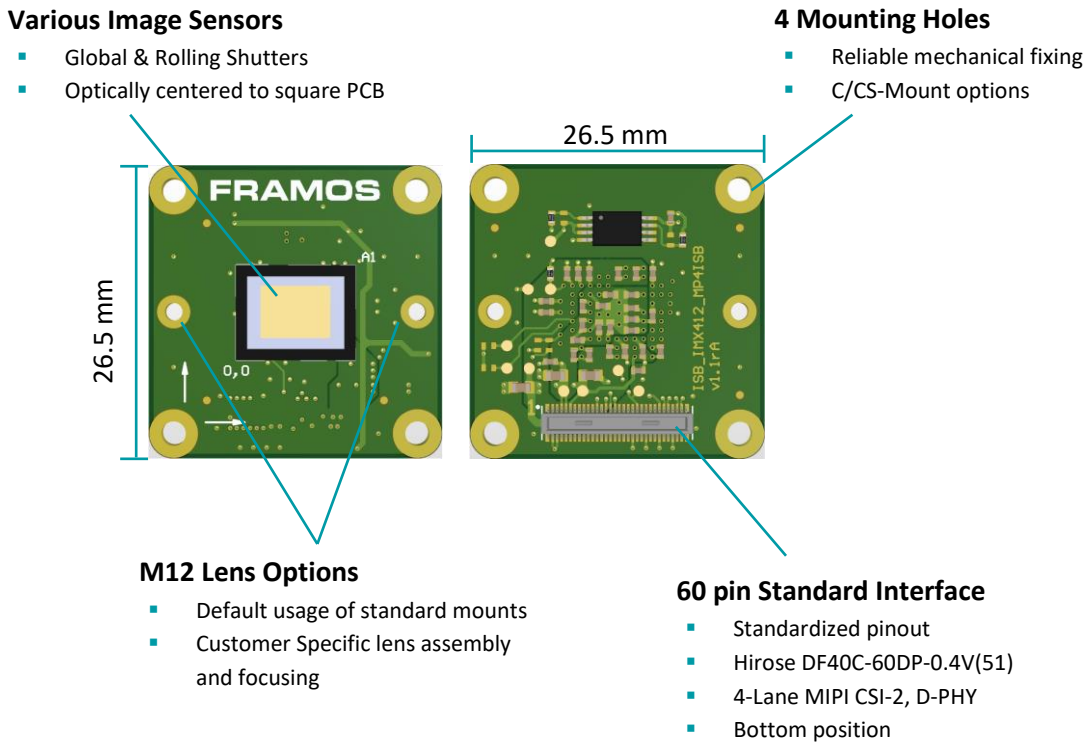
Common Specification

In general, FSMs are differentiated by two main attributes:

- Image sensor size dependent mechanical footprint (26.5 mm, 28 mm)
- Data interface type specific pinout (MIPI CSI-2, LVDS)

All image sensor signals are routed directly from sensor to the 60-pin connector. All passives visible on the PCB decouple the various power loads of the image sensor. Please refer to the appropriate image sensor documentation for further information.

3.1.1 Generic 26.5 mm footprint



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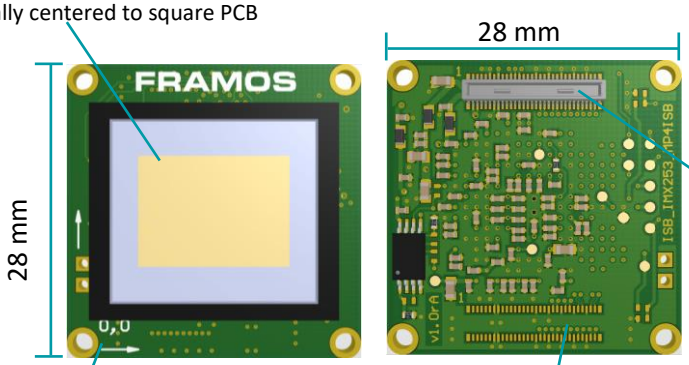
3.1.2 Generic 28 mm footprint

Various Image Sensors ≥2/3”

- Focus on industrial Global Shutters
- Optically centered to square PCB



60 pin Standard Interface

- Standardized pinout
- Hirose DF40C-60DP-0.4V(51)
- Up to 8-Lane Sub-LVDS, SLVS or SLVS-EC output
- MIPI CSI-2 converter options
- Top position

4 Mounting Holes

- Reliable fixing
- C/CS-Mount options

Second Connector Optional

- Hirose DF40C-60DP-0.4V(51)
- Support for 16 Lane LVDS (8+8 Lanes)
- Bottom position

3.2 Connector Pinouts

The FSM Ecosystem adopts a standard Hirose 60 pin board to board connector supporting 5Gbps and beyond, to connect to all relevant signals from the image sensor.

- Connector Type (All FSM): Hirose DF40C-60DP-0.4V
- Number of Pins: 60
- Locking: No
- Shielding: No
- Pinning Layouts:
  - MIPI CSI-2
  - LVDS, SLVS, SLVS-EC

Actual signals used by the individual FSM is image sensor dependent and may vary.

3.2.1 MIPI CSI-2 Pinout (4-Lane)

This pinout scheme applies to all sensors that natively output image data according to the MIPI CSI-2 standard. As by the definition in the MIPI standard, this layout provides 1x4 or 2x2 data lanes on the connector.

Pin#	Signal	Pin#	Signal
1	3V8	2	1V8
3	3V8	4	1V8
5	V_ANA	6	V_DIG
7	V_ANA	8	V_DIG
9	V_IF	10	AUX_V
11	GND	12	GND
13	GND	14	GND
15	RST_0	16	RST_1
17	SPI_MISO	18	SPI_MOSI
19	XMASTER0	20	XMASTER1
21	I2C_0_SCL	22	I2C_1_SCL
23	SPI_CS	24	SPI_SCK
25	XVS0	26	XVS1
27	I2C_0_SDA	28	I2C_1_SDA
29	XHS0	30	XHS1
31	XTRIG0	32	XTRIG1
33	PW_EN_0	34	PW_EN_1
35	SLAMODE1	36	SLAMODE2
37	GND	38	GND
39	INCK	40	UART_TXD
41	MCLK_1	42	UART_RXD
43	GND	44	GND
45	D_CLK_1_P	46	D_DATA_3_P
47	D_CLK_1_N	48	D_DATA_3_N
49	GND	50	GND
51	D_DATA_0_N	52	D_DATA_1_N
53	D_DATA_0_P	54	D_DATA_1_P
55	GND	56	GND
57	D_DATA_2_P	58	D_CLK_0_P
59	D_DATA_2_N	60	D_CLK_0_N

Common Voltages (from FPA)
Sensor Specific Voltages (FSA)
Sensor Signals
Driving Clocks
Data Lines

Table 1: Standard Pinout of MIPI CSI-2 (4-Lane) interface

The table above shows the position of each signal on the 60-pin connector in case the image sensor provides it. For further details, please refer to the image sensor Datasheet.

3.2.2 Sub-LVDS, SLVS and SLVS-EC Pinout (8-Lane)

This pinout scheme applies to all sensors that natively output image data using signals according to Sub-LVDS, SLVS or SLVS-EC specification. This layout provides eight data lanes on the connector. Devices with SLVS and SLVS-EC share the same sensor package pins therefore share the same connector pins.

Note: Lane number assignment is applied according to SLVS numbering, which differs in most cases from the SLVS-EC lane numbering. Please refer to image sensor datasheet for correct SLVS-EC numbering.

Pin#	Signal	Pin#	Signal
1	3V8	2	1V8
3	3V8	4	1V8
5	V_ANA	6	V_DIG
7	V_ANA	8	V_DIG
9	V_IF	10	AUX_V
11	GND	12	GND
13	GND	14	GND
15	SDA	16	SCL
17	SDO	18	XCE
19	TOUT0	20	SLAMODE
21	TOUT1	22	XMASTER
23	TOUT2	24	NC
25	NC	26	XTRIG
27	NC	28	XHS
29	NC	30	XVS
31	GND	32	GND
33	RST	34	D_DATA_7_P
35	MCLK	36	D_DATA_7_N
37	GND	38	GND
39	D_DATA_6_P	40	D_DATA_5_P
41	D_DATA_6_N	42	D_DATA_5_N
43	GND	44	GND
45	D_DATA_4_P	46	D_DATA_3_P
47	D_DATA_4_N	48	D_DATA_3_N
49	GND	50	GND
51	D_DATA_2_P	52	D_DATA_1_P
53	D_DATA_2_N	54	D_DATA_1_N
55	GND	56	GND
57	D_DATA_0_P	58	D_CLK_0_P
59	D_DATA_0_N	60	D_CLK_0_N

Common Voltages (from FPA)
Sensor Specific Voltages (FSA)
Sensor Signals
Driving Clock
Data Lines

Table 2: Standard Pinout of LVDS (8-Lane) interface

The table above shows the position of each signal on the 60-pin connector in case the image sensor provides it. For further details, please refer to the image sensor Datasheet.

3.3 Portfolio Overview of Sensor Modules

The portfolio of sensor modules includes several FSMs, which are listed with their main attributes on the following pages:

- Native MIPI CSI-2 Modules – Global Shutters
- Native MIPI CSI-2 Modules – Rolling Shutters
- Sub-LVDS, SLVS and SLVS-EC Modules

These attributes describe the individual FSMs without any additional hardware like FSA or FPA. They are defined by the integration of the bare image sensor and are not manipulated or preprocessed in any way.

3.3.1 Native MIPI CSI-2 Modules

Global Shutters

Model Name	FSM-IMX297	FSM-AR0144	FSM-IMX296	FSM-HDP230
Shutter Type	CMOS Global Shutter	CMOS Global Shutter	CMOS Global Shutter	CMOS Global Shutter
Resolution [MP]	0,4	1	1,6	2,3
Resolution [HxV]	720 x 540	1280 x 800	1440 x 1080	1944 x 1204
Max. Framerate [FPS]	120	60	60	60
Mono / Color	Mono	Color / Mono	Mono	Color / Mono
Sensor Manufacturer	Sony	ON Semiconductor	Sony	Pyxalis
Sensor Name	IMX297LLR / IMX297LQR	AR0144CSSC	IMX296LLR / IMX296LQR	HDPYX 230-G Mono / Color
Optical Format [inch]	1/2.9	1/4	1/2.9	1/2.5
Pixel Size [µm]	6.9 x 6.9	3 x 3	3.45 x 3.45	3.2 x 3.2
Pixel Bitdepth	10 bit	10 /12 bit	10 bit	8 /10 /12 /14 /16 bit
Data Interface [Type]	MIPI CSI-2	MIPI CSI-2	MIPI CSI-2	MIPI CSI-2
Data Interface [# Lanes]	1	1 / 2	1	4
Communication Interface	I²C (4-wire serial)	I²C	I²C (4-wire serial)	I²C
Drive Frequency [MHz]	37.125 / 74.25 / 54	6 to 48	37.125 / 74.25 / 54	6 to 27 MHz
Input Voltages	1.2V, 1.8V, 3.3V	1.2V, 1.8V, 2.8V	1.2V, 1.8V, 3.3V	1.2V, 1.8V, 2.8V
Supported Lens Mounts	M12 or C/CS-Mount options	M12 or C/CS-Mount options	M12 or C/CS-Mount options	M12 or C/CS-Mount options
Board Dimensions	26.5 mm x 26.5 mm	26.5 mm x 26.5 mm	26.5 mm x 26.5 mm	26.5 mm x 26.5 mm

Rolling Shutters (Part 1/2)

Model Name	FSM-IMX327	FSM-IMX290	FSM-IMX462	FSM-IMX464	FSM-IMX335	FSM-AR0521	FSM-IMX334
Shutter Type	CMOS Rolling Shutter	CMOS Rolling Shutter	CMOS Rolling Shutter	CMOS Rolling Shutter	CMOS Rolling Shutter	CMOS Rolling Shutter	CMOS Rolling Shutter
Resolution [MP]	2,1	2,1	2,1	4,2	5	5	8,3
Resolution [HxV]	1920 x 1080	1920 x 1080	1920 x 1080	2712 x 1538	2592 x 1944	2592 x 1944	3840 x 2160
Max. Framerate [FPS]	60	120	120	90	60	60	60
Mono / Color	Color	Mono	Color	Color	Color / Mono	Color / Mono	Color / Mono
Sensor Manufacturer	Sony	Sony	Sony	Sony	Sony	ON Semiconductor	Sony
Sensor Name	IMX327LQR	IMX290LLR / IMX290LQR	IMX462LQR	IMX464LQR	IMX335LQN / IMX335LLN	AR0521SR2C / AR0521SR2M	IMX334LQR / IMX334LLR
Optical Format [inch]	1/2.8	1/2.8	1/2.8	1/1.8	1/2.8	1/2.5	1/1.8
Pixel Size [µm]	2.9 x 2.9	2.9 x 2.9	2.9 x 2.9	2.9 x 2.9	2 x 2	2.2 x 2.2	2 x 2
Pixel Bitdepth	10 / 12 bit	10 /12 bit	10 /12 bit	10 /12 bit	10 / 12 bit	8 / 10 / 12 bit	10 / 12 bit
Data Interface [Type]	MIPI CSI-2	MIPI CSI-2	MIPI CSI-2	MIPI CSI-2	MIPI CSI-2	MIPI CSI-2	MIPI CSI-2
Data Interface [# Lanes]	2 / 4	2 / 4	2 / 4	2 / 4	2 / 4	4	4
Communication Interface	I²C (4-wire serial)	I²C (4-wire serial)	I²C	I²C	I²C	I²C	I²C
Drive Frequency [MHz]	37.125 / 74.25	37.125 / 74.25	37.125 / 74.25	6 to 27 / 37.125 / 74.25	6 - 27 / 37.125 / 74.25	10 - 48	6 - 27 / 37.125 / 74.25 / 54
Input Voltages	1.2V, 1.8V, 2.9V	1.2V, 1.8V, 2.9V	1.2V, 1.8V, 2.9V	1.2V, 1.8V, 2.9V	1.2V, 1.8V, 2.9V	1.2V, 1.8V, 2.7V	1.2V, 1.8V, 2.9V
Supported Lens Mounts	M12 or C/CS-Mount options	M12 or C/CS-Mount options	M12 or C/CS-Mount options	M12 or C/CS-Mount options	M12 or C/CS-Mount options	M12 or C/CS-Mount options	M12 or C/CS-Mount options
Board Dimensions	26.5 mm x 26.5 mm	26.5 mm x 26.5 mm	26.5 mm x 26.5 mm	26.5 mm x 26.5 mm	26.5 mm x 26.5 mm	26.5 mm x 26.5 mm	26.5 mm x 26.5 mm

Rolling Shutters (Part 2/2)

Model Name	FSM-IMX485	FSM-IMX415	FSM-IMX412	FSM-IMX577	FSM-IMX477	FSM-AR1335	FSM-IMX283
Shutter Type	CMOS Rolling Shutter	CMOS Rolling Shutter	CMOS Rolling Shutter	CMOS Rolling Shutter	CMOS Rolling Shutter	CMOS Rolling Shutter	CMOS Rolling Shutter
Resolution [MP]	8,3	8,4	12,3	12,3	12,3	13,1	20,2
Resolution [HxV]	3840 x 2160	3864 x 2176	4056 x 3040	4056 x 3040	4056 x 3040	4208 x 3120	5496 x 3672
Max. Framerate [FPS]	60	90	60	60	60	30	25
Mono / Color	Color	Color	Color	Color	Color	Color	Color
Sensor Manufacturer	Sony	Sony	Sony	Sony	Sony	ON Semiconductor	Sony
Sensor Name	IMX485LQJ	IMX415-AAQR	IMX412-AACK	IMX577-AACK	IMX477-AACK	AR1335CSSC	IMX283CQJ
Optical Format [inch]	1/1.2	1/2.8	1/2.3	1/2.3	1/2.3	1/3.2	1
Pixel Size [µm]	2.9 x 2.9	1.45 x 1.45	1.55 x 1.55	1.55 x 1.55	1.55 x 1.55	1.1 x 1.1	2.4 x 2.4
Pixel Bitdepth	10 /12 bit	10 /12 bit	10 / 12 bit	8 / 10 / 12 bit	8 / 10 / 12 bit	10 bit	10 /12 bit
Data Interface [Type]	MIPI CSI-2	MIPI CSI-2	MIPI CSI-2	MIPI CSI-2	MIPI CSI-2	MIPI CSI-2	MIPI CSI-2
Data Interface [# Lanes]	2 / 4 (/ 8)	2 / 4	2 / 4	2 / 4	2 / 4	2 / 4	4
Communication Interface	I²C	I²C	I²C (CCI)	I²C (CCI)	I²C (CCI)	I²C	I²C
Drive Frequency [MHz[	6 to 27 / 37.125 / 74.25	24 / 27 / 37.125 / 72 / 74.25	6 / 12 / 18 / 24 / 27	6 to 27	6 to 27	6 to 48	6 to 27
Input Voltages	1.2V, 1.8V, 2.9V	1.1V, 1.8V, 2.9V	1.05V, 1.8V, 2.75V	1.05V, 1.8V, 2.8V	1.05V, 1.8V, 2.8V	1.2V, 1.8V, 2.7V	1.2V, 1.8V, 2.9V
Supported Lens Mounts	C/CS-Mount option	M12 or C/CS-Mount options	M12 or C/CS-Mount options	M12 or C/CS-Mount options	M12 or C/CS-Mount options	M12 or C/CS-Mount options	C/CS-Mount
Board Dimensions	26.5 mm x 26.5 mm	26.5 mm x 26.5 mm	26.5 mm x 26.5 mm	26.5 mm x 26.5 mm	26.5 mm x 26.5 mm	26.5 mm x 26.5 mm	26.5 mm x 26.5 mm

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3.3.2 Sub-LVDS, SLVS and SLVS-EC Modules

Model Name	FSM-IMX264	FSM-IMX304	FSM-IMX530
Shutter Type	CMOS Global Shutter	CMOS Global Shutter	CMOS Global Shutter
Resolution [MP]	5,1	12,4	24,5
Resolution [HxV]	2464 x 2056	4112 x 3008	5320 x 4600
Max. Framerate [FPS]	35	23	98
Mono / Color	Color / Mono	Color / Mono	Color / Mono
Sensor Manufacturer	Sony	Sony	Sony
Sensor Name	IMX264LLR / IMX264LQR	IMX304LQR / IMX304LLR	IMX530-AAMJ / IMX530-AAQJ
Optical Format [inch]	2/3	1.1	1.2
Pixel Size [µm]	3.45 x 3.45	3.45 x 3.45	2.74 x 2.74
Pixel Bitdepth	12 bit	12 bit	8 /10 /12 bit
Data Interface [Type]	Sub-LVDS	Sub-LVDS	SLVS, SLVS-EC
Data Interface [# Lanes]	4	4 / 8	1 /2 /4/ 8
Communication Interface	I^2C (4-wire serial)	I^2C (4-wire serial)	I^2C (4-wire serial)
Drive Frequency [MHz]	37.125 / 54 / 74.25	37.125 / 54 / 74.25	37.125 / 54 / 74.25
Input Voltages	1.2V, 1.8V, 3.3V	1.2V, 1.8V, 3.3V	1.1V, 1.8V, 2.9V, 3.3V
Supported Lens Mounts	C/CS-Mount option	C/CS-Mount	C/CS-Mount option
Board Dimensions	28 mm x 28 mm	28 mm x 28 mm	28 mm x 28 mm

4 Ecosystem for Sub-LVDS, SLVS and SLVS-EC Image Sensors

The following chapters provide the relevant technical information for Sub-LVDS, SLVS and SLVS-EC sensor modules (FSM), according to the two supported data chains:

- Data conversion to MIPI CSI-2
- Native data streaming

4.1 Sub-LVDS and SLVS Sensors on MIPI CSI-2

The Sub-LVDS and SLVS sensor setup with MIPI CSI-2 conversion hardware configuration consists of one or multiple FSMs with Sub-LVDS or SLVS output, each with an appropriate sensor specific FSA and one FPA for the target processor board. The MIPI CSI-2 conversion takes place on the FSA. Only FSA and FPA designs shown in this chapter are compatible to each other. The FPA defines the maximum number of sensor modules that can be operated per processor board.

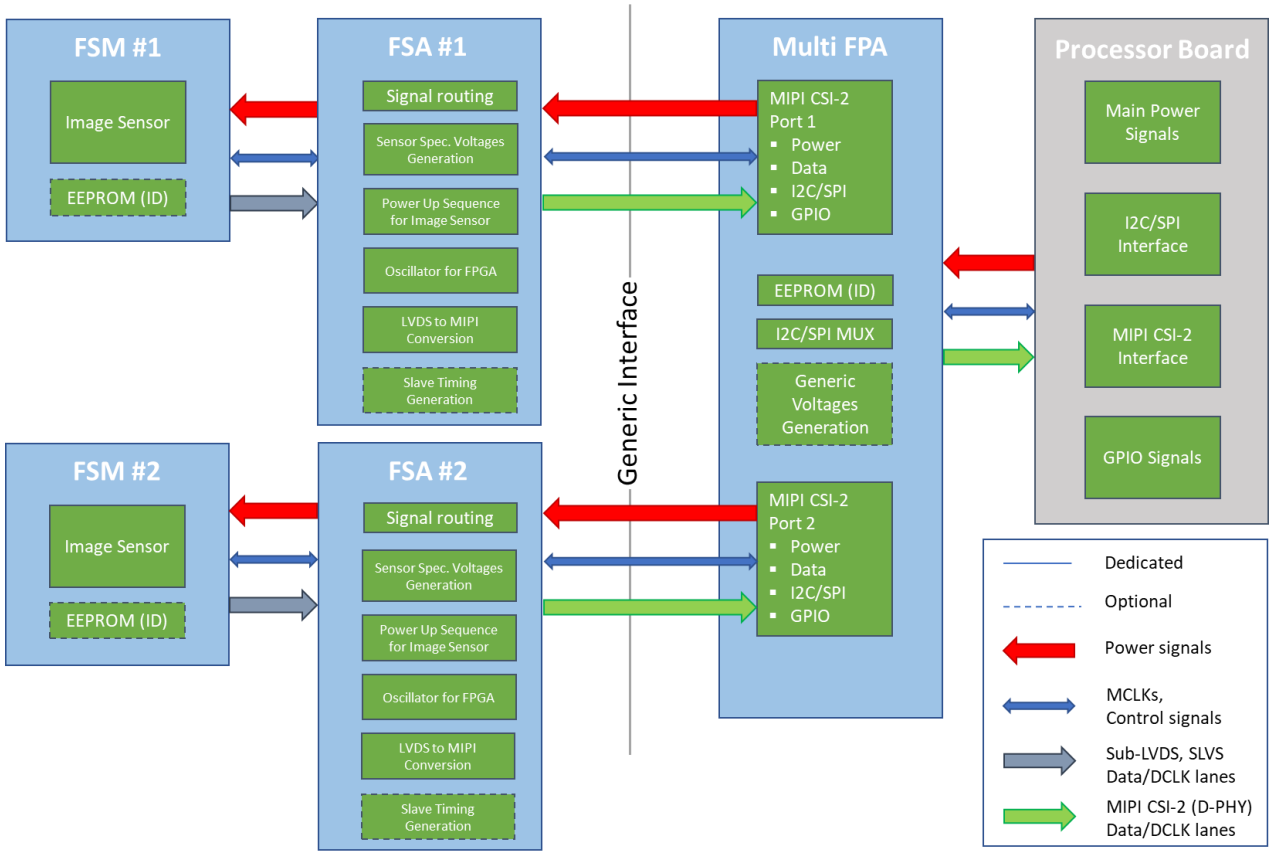


Figure 3: Block Diagram of components in Sub-LVDS / SLVS to MIPI CSI-2 Sensor Setup

4.2 Pure Sub-LVDS, SLVS or SLVS-EC Chain

The pure Sub-LVDS, SLVS and SLVS-EC sensor setup consists of one or multiple FSMs with Sub-LVDS or SLVS output, each with an appropriate sensor specific FSA and one FPA for the target processor board. No data signal conversion takes place. Only FSA and FPA designs shown in this chapter are compatible to each other. The FPA defines the maximum number of sensor modules that can be operated per processor board.

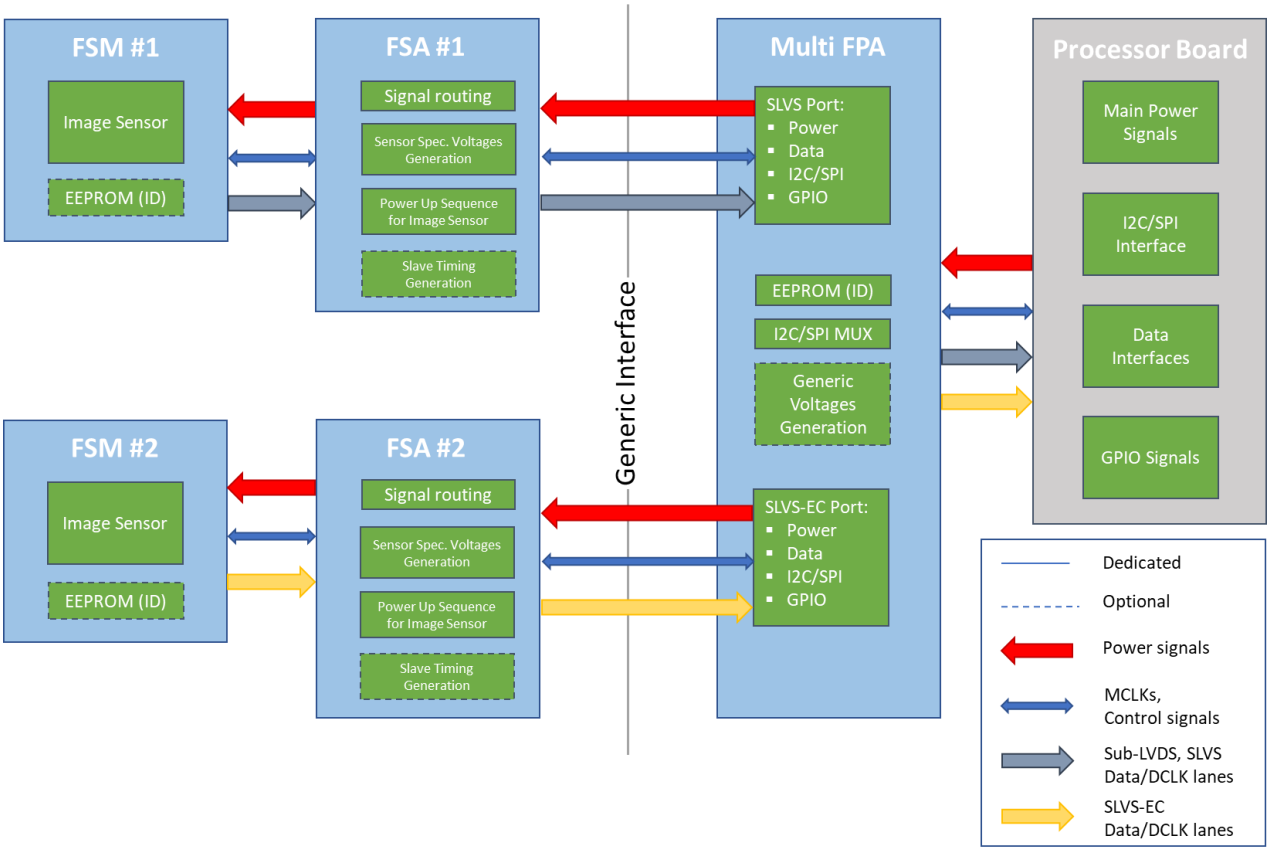
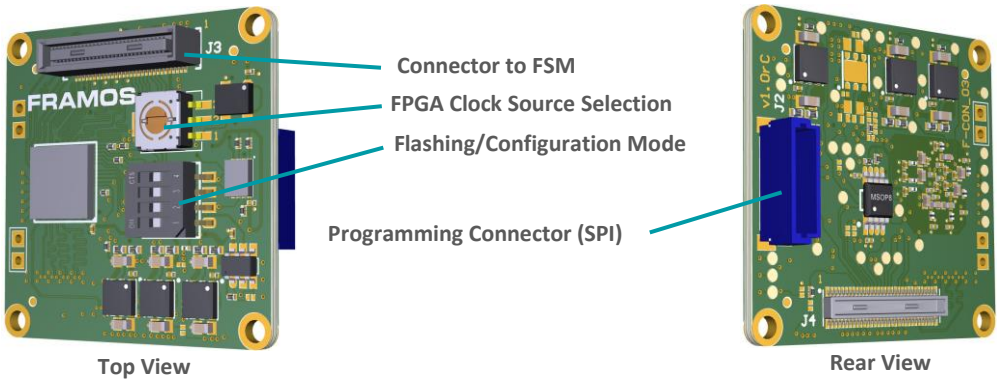


Figure 4: Block Diagram of components in Sub-LVDS, SLVS and SLVS-EC Sensor Setup

5 FSA-FTx/A-00G: FRAMOS Sensor Adapter with LVDS to MIPI Conversion Bridge

- Connects FSM with Sub-LVDS or SLVS data output to FPA with MIPI CSI-2 input
- Performs image data conversion to MIPI CSI-2 (D-PHY)
- Each FSA variant ("x") might be FSM specific



Functional Blocks:

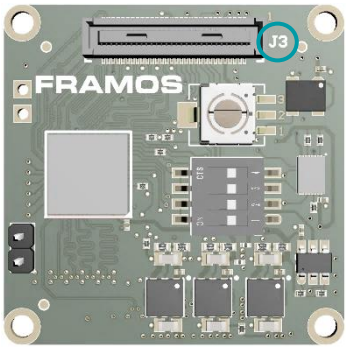
- Signal routing
- Voltage generation and up sequence for image sensor
- Master clock and slave timing generation
- Image data conversion to MIPI CSI-2

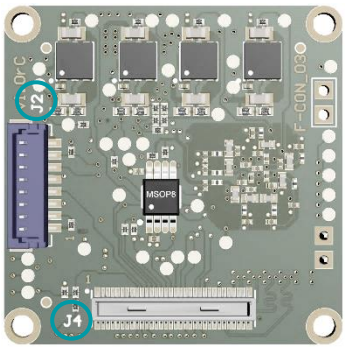
5.1 Functional Specification

Item	FSA-FT14/A-00G	FSA-FT15/A-00G	FSA-FT18/A-00G
Supported FSM	FSM-IMX264	FSM-IMX304	FSM-IMX530
Color / Mono	Both		
Resolution & Framerate	**2448 x 2048 @ 35FPS** 2048 x 1536 @ 47FPS 1920 x 1080 @ 60FPS	**4096 x 3000 @ 23FPS** 4096 x 2160 @ 30FPS 3840 x 2160 @ 30FPS	**5320 x 4600 @ 15FPS** 4512 x 4512 @ 18FPS 5328 x 3040 @ 22FPS 4064 x 3008 @ 27FPS 2660 x 2300 @ 54FPS
Bit Depth[1]	10, 12 bit (RAW)		
Input Data Format	4-Lane, Sub-LVDS	8-Lane, Sub-LVDS	8-Lane, SLVS
Output Data Format	4-Lane, MIPI CSI-2 (D-PHY) @ 594 Mbps	4-Lane, MIPI CSI-2 (D-PHY) @ 1.2 Gbps	4-Lane, MIPI CSI-2 (D-PHY) @ 594 Mbps
Operating Mode	Master, Slave		
Clock Source	Internal (37.125MHz), or extern via processor board		
FW Upgrade[1]	I2C (int), SPI (ext)		
Driver	NVIDIA Jetson TX2, AGX Xavier (LibSV and Libargus)		

[1] Firmware updates are applied via the processor board over the I2C bus, or using the external SPI interface attaching an appropiate programmer (Lattice HW-USBN-2B). Updates to the onboard flash are permanent and can only be applied via SPI. Updates via I2C will be lost when powercycling the FSA.

5.2 Interface Description



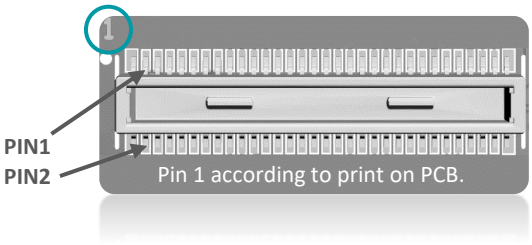


5.2.1 J3: Connector to FSM

Label: J3
Type: DF40HC(4.0)-60DS-0.4V
Pinout: According to FSM

5.2.2 J4: Connector to FPA

Label: J4
Type: DF40C-60DP-0.4V
Pinout:



Pin #	Name	Pin #	Name
1	3V8_VDD	2	1V8_VDD
3	3V8_VDD	4	1V8_VDD
5	NC	6	NC
7	NC	8	NC
9	NC	10	NC
11	GND	12	GND
13	GND	14	GND
15	RST_0	16	RST_1
17	EE_MISO	18	GPIO15(SPI_MISO)
19	GPIO0(XMASTER0)	20	EE_MOSI
21	I2C_0_SCL(SPI_SCK)	22	NC
23	GPIO17(SPI_CS)	24	GPIO16(SYS_PW_EN)
25	GPIO1(XVS0)	26	EE_SCK
27	I2C_0_SDA(SPI_MOSI)	28	NC
29	GPIO2(XHS0)	30	EE_SS
31	GPIO3(XTRIG0)	32	GPIO11
33	PW_EN	34	CRESET_B
35	GPIO6	36	GPIO7
37	GND	38	GND
39	MCLK_0	40	GPIO4(MCLK2)
41	MCLK_1	42	GPIO5(MCLK3)
43	GND	44	GND
45	NC	46	D_DATA_3_P
47	NC	48	D_DATA_3_N
49	GND	50	GND
51	D_DATA_0_N	52	D_DATA_1_N
53	D_DATA_0_P	54	D_DATA_1_P
55	GND	56	GND
57	D_DATA_2_P	58	D_CLK_0_P
59	D_DATA_2_N	60	D_CLK_0_N

Table 3: Pinout of FSA-FTx/A-00G-V1, connector to FRAMOS Processor Adapter (FPA)

J4: Signal Description (Part 1/2)

Pin	Net name	I/O	Primary function description	Connected to	I/O Standard	I/O State	I/O DC Characteristic
1	3V8_VDD	Power	3.8V Power Supply	LDO_ICs, FSM			3V8_VDD=3.7V-5.1V
2	1V8_VDD	Power	1.8V Power Supply	LDO_ICs, FSM			1V8_VDD=1.7V-1.9V
3	3V8_VDD	Power	3.8V Power Supply	LDO_ICs, FSM			3V8_VDD=3.7V-5.1V
4	1V8_VDD	Power	1.8V Power Supply	LDO_ICs, FSM			1V8_VDD=1.7V-1.9V
5	NC	-	Not Connected				
6	NC	-	Not Connected				
7	NC	-	Not Connected				
8	NC	-	Not Connected				
9	NC	-	Not Connected				
10	NC	-	Not Connected				
11	GND	GND	Common Ground				
12	GND	GND	Common Ground				
13	GND	GND	Common Ground				
14	GND	GND	Common Ground				
15	RST_0	IN	General reset for FSA and FSM, resets Crosslink logic and image sensor (XCLR).	Reset_IC	LVCMOS18 (1.8V)	Normal: High, Reset: Low	VILmax=0.36V,VIHmin=1.44V
16	RST_1	IN		Reset_IC	LVCMOS18 (1.8V)	Normal: High, Reset: Low	VILmax=0.36V,VIHmin=1.44V
17	EE_MISO	OUT	4-wire SPI MISO for Crosslink and Flash programming	CrossLink, Flash	LVCMOS18 (1.8V)		VOLmax=0.2V,VOHmin=1.6V
18	GPIO15(SPI_MISO)	OUT		FSM	LVCMOS18 (1.8V)		VOLmax=0.2V,VOHmin=1.6V
19	GPIO0(XMASTER0)	IN/OUT	Connected to Test Point (TP22)	Test point			
20	EE_MOSI	IN	4-wire SPI MOSI for Crosslink and Flash programming	CrossLink, Flash	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin=1.44V
21	I2C_0_SCL(SPI_SCK)	IN	I2C SCL for Crosslink user interface and FSM	CrossLink, FSM	LVCMOS18 (1.8V)		VILmax=0.54V,VIHmin=1.26V
22	NC	-	Not Connected				
23	GPIO17(SPI_CS)	IN		FSM	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin=1.44V
24	GPIO16(SYS_PW_EN)	IN/OUT	Connected to Test Point (TP34)	Test point, FSM	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin=1.44V
25	GPIO1(XVS0)	IN/OUT	Multiple FSM synchronization	CrossLink	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin=1.44V VOLmax=0.2V,VOHmin=1.6V
26	EE_SCK	IN	4-wire SPI SCK for Crosslink and Flash programming	CrossLink, Flash	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin=1.44V
27	I2C_0_SDA (SPI_MOSI)	IN/OUT	I2C SDA for Crosslink user interface and FSM	CrossLink, FSM	LVCMOS18 (1.8V)		VILmax=0.54V,VIHmin=1.26V VOLmax=0.36V,VOHmin=1.44V
28	NC	-	Not Connected				
29	GPIO2(XHS0)	IN/OUT	Connected to Test Point (TP23)	Test point			
30	EE_SS	IN	4-wire SPI CS for Crosslink and Flash programming	CrossLink, Flash	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin=1.44V
31	GPIO3(XTRIG0)	IN/OUT	Connected to Test Point (TP24)	Test point			
32	GPIO11	OUT		FSM	LVCMOS18 (1.8V)		VOLmax=0.2V,VOHmin=1.6V
33	PW_EN	IN	FSA Power Enable (Crosslink and FSM)	LDO_ICs	LVCMOS18 (1.8V)	Normal: High, Pwr Down: Low	VILmax=0.36V,VIHmin=1.44V
34	CRESET_B	IN	Reset Crosslink Configuration	CrossLink	LVCMOS18 (1.8V)	Normal: High, Reset: Low	VILmax=0.36V,VIHmin=1.44V

J4: Signal Description (Part 2/2)

Pin	Net name	I/O	Primary function description	Connected to	I/O Standard	I/O State	I/O DC Characteristic
35	GPIO6	IN/OUT	Connected to Test Point (TP21)	Test point, (FSM)	LVCMOS18 (1.8V)	1A: High, 10: Low	VILmax=0.36V,VIHmin=1.44V
36	GPIO7	IN/OUT	Connected to Test Point (TP33)	Test point			
37	GND	GND	Common Ground				
38	GND	GND	Common Ground				
39	MCLK_0	IN CLK	Master clock 0 (Crosslink input clock when SW2 in position 2)	Rotary Switch	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin=1.44V
40	GPIO4(MCLK2)	IN/OUT	Connected to Test Point (TP32)	Test point			
41	MCLK_1	IN CLK	Master clock 1 (Crosslink input clock when SW2 in position 3)	Rotary Switch	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin=1.44V
42	GPIO5(MCLK3)	IN/OUT	Connected to Test Point (TP31)	Test point			
43	GND	GND	Common Ground				
44	GND	GND	Common Ground				
45	NC	-	Not Connected				
46	D_DATA_3_P	OUT	MIPI-CSI2 output data (3, P)	CrossLink	MIPI D-PHY		
47	NC	-	Not Connected				
48	D_DATA_3_N	OUT	MIPI-CSI2 output data (3, N)	CrossLink	MIPI D-PHY		
49	GND	GND	Common Ground				
50	GND	GND	Common Ground				
51	D_DATA_0_N	OUT	MIPI-CSI2 output data (0, N)	CrossLink	MIPI D-PHY		
52	D_DATA_1_N	OUT	MIPI-CSI2 output data (1, N)	CrossLink	MIPI D-PHY		
53	D_DATA_0_P	OUT	MIPI-CSI2 output data (0, P)	CrossLink	MIPI D-PHY		
54	D_DATA_1_P	OUT	MIPI-CSI2 output data (1, P)	CrossLink	MIPI D-PHY		
55	GND	GND	Common Ground				
56	GND	GND	Common Ground				
57	D_DATA_2_P	OUT	MIPI-CSI2 output data (2, P)	CrossLink	MIPI D-PHY		
58	D_CLK_0_P	OUT CLK	MIPI-CSI2 output clock (0, P)	CrossLink	MIPI D-PHY		
59	D_DATA_2_N	OUT	MIPI-CSI2 output data (2, N)	CrossLink	MIPI D-PHY		
60	D_CLK_0_N	OUT CLK	MIPI-CSI2 output clock (0, N)	CrossLink	MIPI D-PHY		

5.2.3 Firmware Flashing/Configuration

Options \ Switch Pattern	1	2	3	4
Boot configuration from flash, configuration and flash update via SPI enabled **(Default)**	**Off**	**On**	**Off**	**On**
Configuration from host via I2C	**On**	**Off**	**On**	**Off**

Table 4: Selection of Sensor Mode on FSA-FTx/A-00G-V1

5.2.4 FPGA Clock Source Selection

Pos.	Description
1	Clock provided from FSA **(Default)**
2	External clock 1 (MCLK0)
3	External clock 2 (MCLK1)

Table 5: Selection of Sensor Clock Source on FSA-FTx/A-00G-V1

5.2.5 Test Points

Name	Signal	Name	Signal	Name	Signal
TP1	PW_EN1	**TP13**	IS_MCLK	**TP25**	XTRIG2
TP2	AUX_V_ANA	**TP14**	GND	**TP26**	GPIO11(TOUT0)
TP3	GND	**TP15**	XHS	**TP27**	GPIO8(TOUT1)
TP4	PW_EN2	**TP16**	IS_RST	**TP28**	GPIO9(TOUT2)
TP5	AUX_V	**TP17**	GND	**TP29**	GPIO16
TP6	GND	**TP18**	XMASTER	**TP30**	GND
TP7	PW_EN3	**TP19**	XVS	**TP31**	GPIO5(MCLK3)
TP8	AUX_V_DIG	**TP20**	GND	**TP32**	GPIO4(MCLK2)
TP9	PW_EN4	**TP21**	GPIO6	**TP33**	GPIO7
TP10	AUX_V_IF1	**TP22**	GPIO0(XMASTER0)	**TP34**	GPIO16(SYS_PW_EN)
TP11	GPIO1(XVS0)	**TP23**	GPIO2(XHS0)		
TP12	XTRIG	**TP24**	GPIO3(XTRIG)		

Table 6: Test Points on FSA-FTx/A-00G-V1

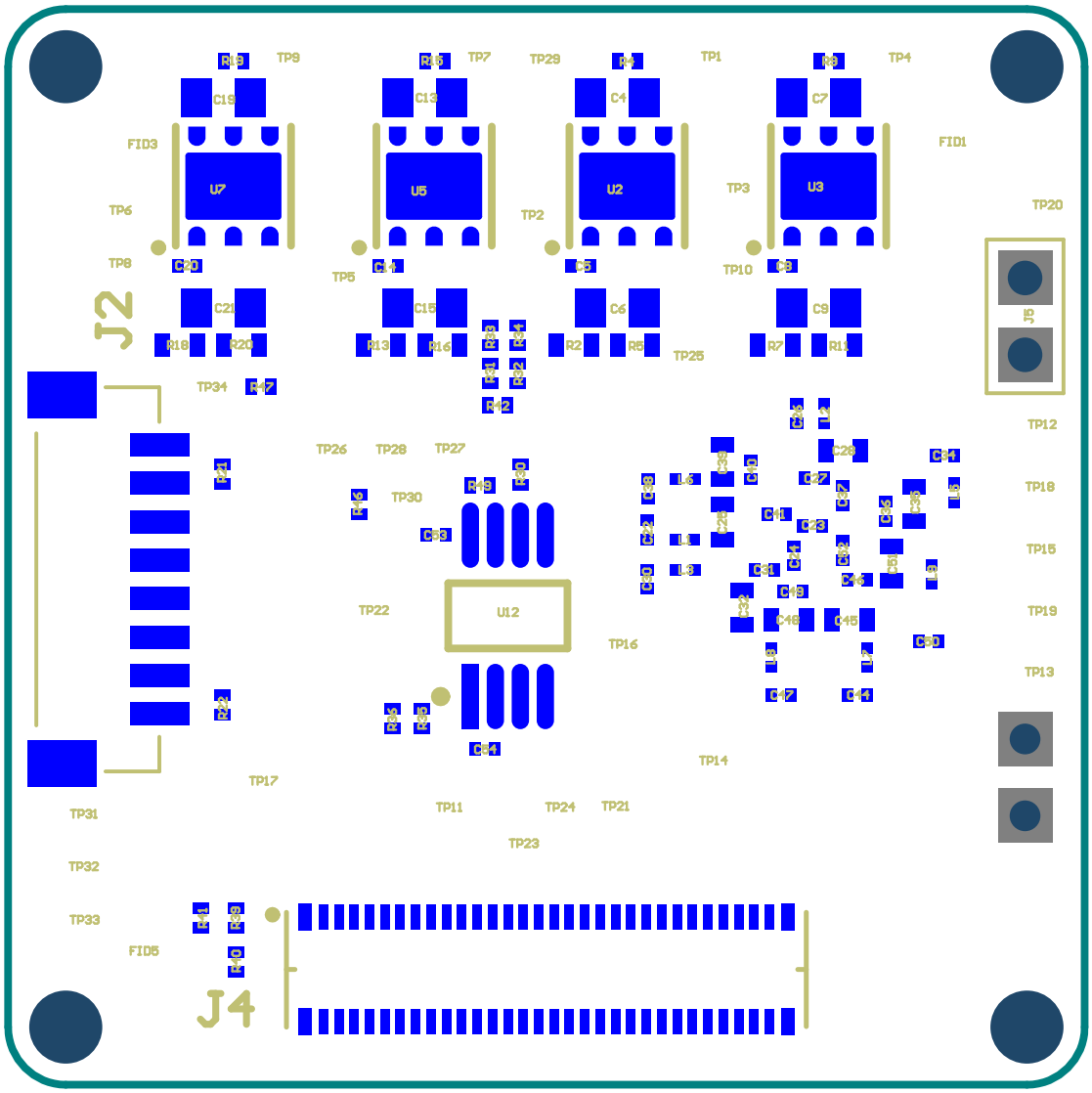
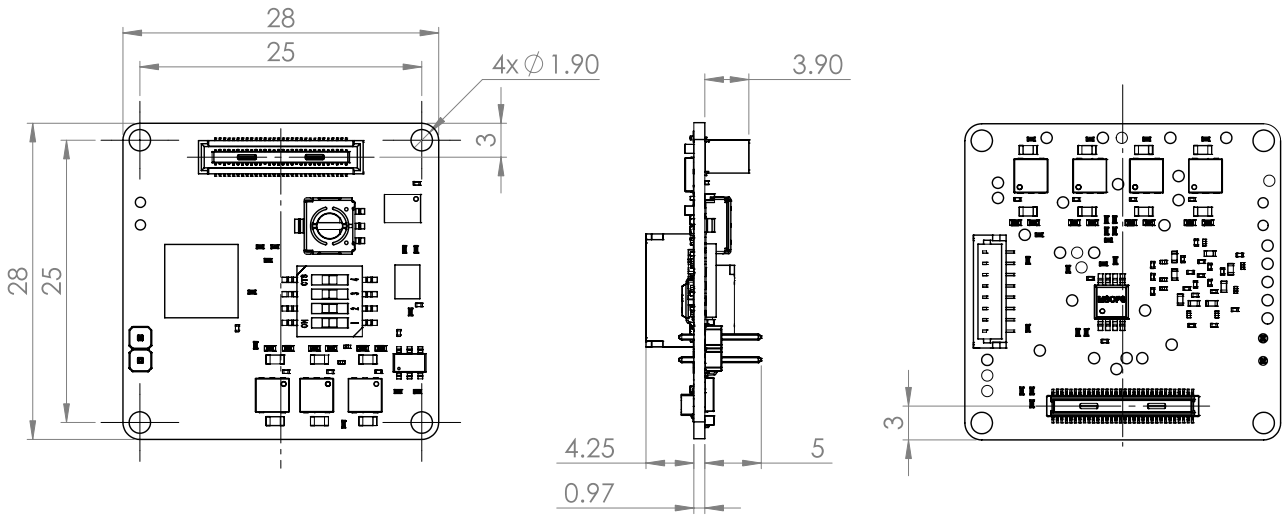


Figure 5: Test Points on FSA-FTx/A-00G-V1

5.3 Technical Drawing



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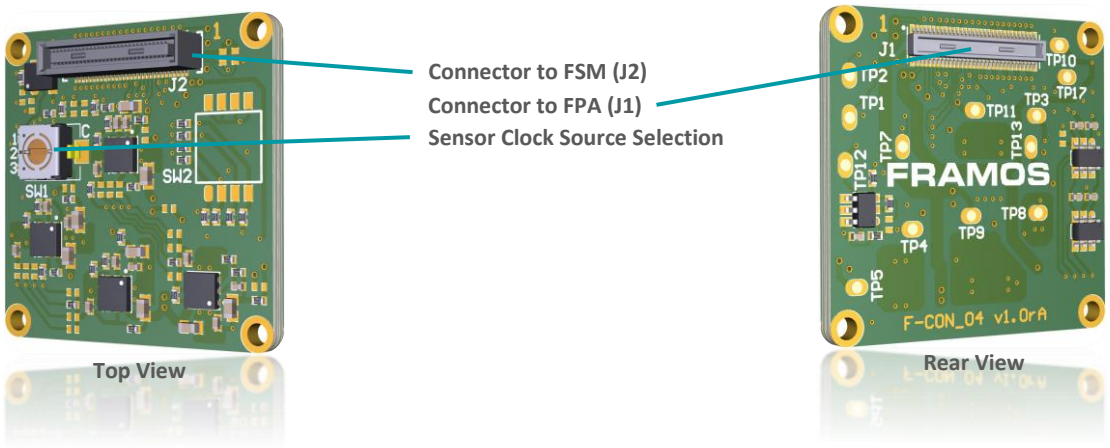
6 FSA-FTx/BC: FRAMOS Sensor Adapter for Sub-LVDS, SLVS and SLVS-EC

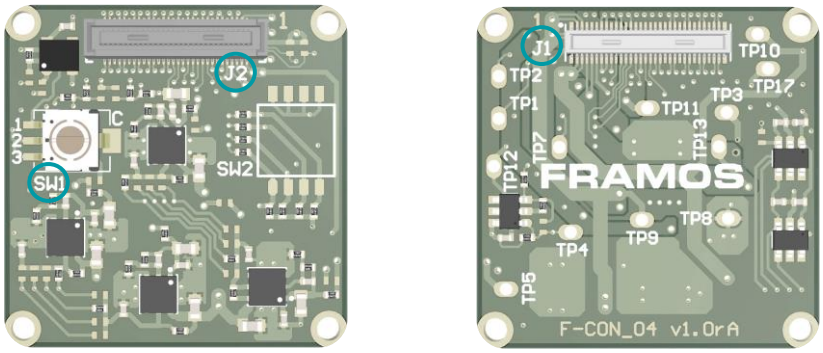
- Connects FSM with Sub-LVDS, SLVS or SLVS-EC output to FPA
- Each FSA variant (“x”) might be FSM specific



Functional Blocks:

- Signal routing
- Voltage generation for image sensor
- Power up sequence for image sensor

6.1 Interface Description



6.1.1 SW1: Sensor Clock Source Selection

Pos.	Description
1	Clock Provided from FSA **(Default)**
2	External Clock 1 (MCLK0)
3	External Clock 2 (MCLK1)

Table 7: Selection of Sensor Clock Source on FSA-FTx/A-V1

6.1.2 J2: Connector to FSM

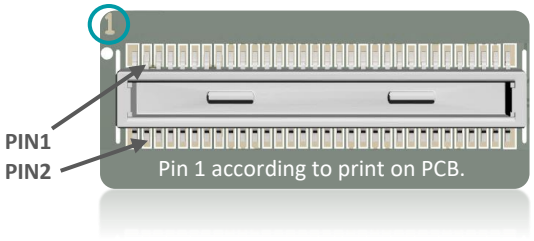
Label: J2
Type: DF40HC(4.0)-60DS-0.4V
Pinout: According to FSM

6.1.3 J1: Connector to FPA

Label: J1

Type: Hirose DF40C-60DP-0.4V

Pinout:



Pin #	Name	Pin #	Name
1	3V8_VDD	2	1V8_VDD
3	3V8_VDD	4	1V8_VDD
5	AUX_ANA	6	AUX_DIG
7	AUX_ANA	8	AUX_DIG
9	AUX_IF	10	AUX_V
11	GND	12	GND
13	GND	14	GND
15	I2C_0_SDA(SPI_MOSI)	16	I2C_0_SCL(SPI_SCK)
17	SDO	18	XCE
19	TOUT0	20	GPIO6
21	TOUT1	22	GPIO0(XMASTER)
23	TOUT2	24	GPIO7
25	GPIO16	26	XTRIG1
27	GPIO14	28	XHS
29	GPIO10	30	XVS
31	GND	32	GND
33	RST_0	34	D_DATA_7_P
35	MCLK_0	36	D_DATA_7_N
37	GND	38	GND
39	D_DATA_6_P	40	D_DATA_5_P
41	D_DATA_6_N	42	D_DATA_5_N
43	GND	44	GND
45	D_DATA_4_P	46	D_DATA_3_P
47	D_DATA_4_N	48	D_DATA_3_N
49	GND	50	GND
51	D_DATA_2_P	52	D_DATA_1_P
53	D_DATA_2_N	54	D_DATA_1_N
55	GND	56	GND
57	D_DATA_0_P	58	D_CLK_0_P
59	D_DATA_0_N	60	D_CLK_0_N

Table 8: Pinout of FSA-FTx/BC-V1, connector to FRAMOS Processor Adapter (FPA) with Sub-LVDS, SLVS or SLVS-EC input

J1: Signal Description (Part 1/2)

Pin	Net name	I/O	Primary function description	Connected to	I/O Standard	I/O State	I/O DC Characteristic
1	3V8_VDD	Power	3.8V Power Supply	LDO_ICs, FSM			3V8_VDD=3.7V-5.1V
2	1V8_VDD	Power	1.8V Power Supply	LDO_ICs, FSM			1V8_VDD=1.7V-1.9V
3	3V8_VDD	Power	3.8V Power Supply	LDO_ICs, FSM			3V8_VDD=3.7V-5.1V
4	1V8_VDD	Power	1.8V Power Supply	LDO_ICs, FSM			1V8_VDD=1.7V-1.9V
5	AUX_V_ANA	Power	Not Connected	(FSM)			
6	AUX_V_DIG	Power	Not Connected	(FSM)			
7	AUX_V_ANA	Power	Not Connected	(FSM)			
8	AUX_V_DIG	Power	Not Connected	(FSM)			
9	AUX_V_IF1	Power	Not Connected	(FSM)			
10	AUX_V	Power	Not Connected	(FSM)			
11	GND	GND	Common Ground				
12	GND	GND	Common Ground				
13	GND	GND	Common Ground				
14	GND	GND	Common Ground				
15	I2C_0_SDA(SPI_MOSI)	IN/OUT	I2C SDA for FSM. Connected to Test Point (TP1)	Test point, FSM	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin= 1.44V, VOLmax=0.4V, VOHmin=1.4V
16	I2C_0_SCL(SPI_SCK)	IN	I2C SCL for FSM. Connected to Test Point (TP2)	Test point, FSM	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin= 1.44V
17	SDO	OUT		FSM	LVCMOS18 (1.8V)		VOLmax=0.4V, VOHmin=1.4V
18	XCE	IN		FSM	LVCMOS18 (1.8V)	I2C: High, 4-wire: Low	VILmax=0.36V, VIHmin= 1.44V
19	TOUT0	OUT	TOUT0 from FSM	FSM	LVCMOS18 (1.8V)		VOLmax=0.4V, VOHmin=1.4V
20	GPIO6	IN	Slave address select for FSM (SLAMODE0)	FSM	LVCMOS18 (1.8V)	1A: High, 10: Low	VILmax=0.36V,VIHmin= 1.44V
21	TOUT1	OUT	TOUT1 from FSM	FSM	LVCMOS18 (1.8V)		VOLmax=0.4V, VOHmin=1.4V
22	GPIO0(XMASTER)	IN	XMASTER for FSM. Connected to Test Point (TP7)	Test point, FSM	LVCMOS18 (1.8V)	Slave: High, Master: Low	VILmax=0.36V, VIHmin= 1.44V
23	TOUT2	OUT	TOUT2 from FSM	FSM	LVCMOS18 (1.8V)		VOLmax=0.4V, VOHmin=1.4V
24	GPIO7	IN	XTRIG2 for FSM	FSM	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin= 1.44V
25	GPIO16	IN	Slave address select for FSM (SLAMODE1)	FSM	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin= 1.44V
26	XTRIG1	IN	XTRIG1 for FSM	FSM	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin= 1.44V
27	GPIO14	IN	Slave address select for FSM (SLAMODE2)	FSM	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin= 1.44V
28	XHS	IN/OUT	XHS for FSM	FSM	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin= 1.44V, VOLmax=0.4V, VOHmin=1.4V
29	GPIO10	IN	OMODE for FSM	FSM, (Power Sequencer)	LVCMOS18 (1.8V)	SLVS-EC: High, SLVS: Low	VILmax=0.36V, VIHmin= 1.44V
30	XVS	IN/OUT	Multiple FSM synchronization	FSM	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin= 1.44V, VOLmax=0.4V, VOHmin=1.4V

J1: Signal Description (Part 2/2)

Pin	Net name	I/O	Primary function description	Connected to	I/O Standard	I/O State	I/O DC Characteristic
31	GND	GND	Common Ground				
32	GND	GND	Common Ground				
33	RST_0	IN	General reset for FSM	Reset_IC	LVCMOS18 (1.8V)	Normal: High, Reset: Low	VILmax=0.54V, VIHmin= 1.26V
34	D_DATA_7_P	OUT	LVDS output data (7, P)	FSM	LVDS/SLVS/SLVS-EC		
35	MCLK_0	IN CLK	Master clock 0 (SW1 in pos 2 or 3)	Rotary switch	LVCMOS18 (1.8V)		VILmax=0.36V, VIHmin= 1.44V
36	D_DATA_7_N	OUT	LVDS output data (7, N)	FSM	LVDS/SLVS/SLVS-EC		
37	GND	GND	Common Ground				
38	GND	GND	Common Ground				
39	D_DATA_6_P	OUT	LVDS output data (6, P)	FSM	LVDS/SLVS/SLVS-EC		
40	D_DATA_5_P	OUT	LVDS output data (5, P)	FSM	LVDS/SLVS/SLVS-EC		
41	D_DATA_6_N	OUT	LVDS output data (6, N)	FSM	LVDS/SLVS/SLVS-EC		
42	D_DATA_5_N	OUT	LVDS output data (5, N)	FSM	LVDS/SLVS/SLVS-EC		
43	GND	GND	Common Ground				
44	GND	GND	Common Ground				
45	D_DATA_4_P	OUT	LVDS output data (4, P)	FSM	LVDS/SLVS/SLVS-EC		
46	D_DATA_3_P	OUT	LVDS output data (3, P)	FSM	LVDS/SLVS/SLVS-EC		
47	D_DATA_4_N	OUT	LVDS output data (4, N)	FSM	LVDS/SLVS/SLVS-EC		
48	D_DATA_3_N	OUT	LVDS output data (3, N)	FSM	LVDS/SLVS/SLVS-EC		
49	GND	GND	Common Ground				
50	GND	GND	Common Ground				
51	D_DATA_2_P	OUT	LVDS output data (2, P)	FSM	LVDS/SLVS/SLVS-EC		
52	D_DATA_1_P	OUT	LVDS output data (1, P)	FSM	LVDS/SLVS/SLVS-EC		
53	D_DATA_2_N	OUT	LVDS output data (2, N)	FSM	LVDS/SLVS/SLVS-EC		
54	D_DATA_1_N	OUT	LVDS output data (1, N)	FSM	LVDS/SLVS/SLVS-EC		
55	GND	GND	Common Ground				
56	GND	GND	Common Ground				
57	D_DATA_0_P	OUT	LVDS output data (0, P)	FSM	LVDS/SLVS/SLVS-EC		
58	D_CLK_0_P	OUT	LVDS output clock (0, P)	FSM	LVDS/SLVS/SLVS-EC		
59	D_DATA_0_N	OUT	LVDS output data (0, N)	FSM	LVDS/SLVS/SLVS-EC		
60	D_CLK_0_N	OUT	LVDS output clock (0, N)	FSM	LVDS/SLVS/SLVS-EC		

6.1.4 TPx: Test Points

Name	Signal	Name	Signal	Name	Signal
TP1	I2C_0_SDA (SPI_MOSI)	**TP7**	IS_GPIO0 (XMASTER0)	**TP12**	V_IF
TP2	I2C_0_SCL (SPI_SCK)	**TP8**	GND	**TP13**	V_DIG
TP3	IS_MCLK_0	**TP9**	3V8_VDD	**TP17**	GND
TP4	IS_RST_0	**TP10**	1V8_VDD		
TP5	V_ANA-1	**TP11**	V_ANA		

Table 9: Test Points on FSA-FTx/BC-V1

6.2 Technical Drawing

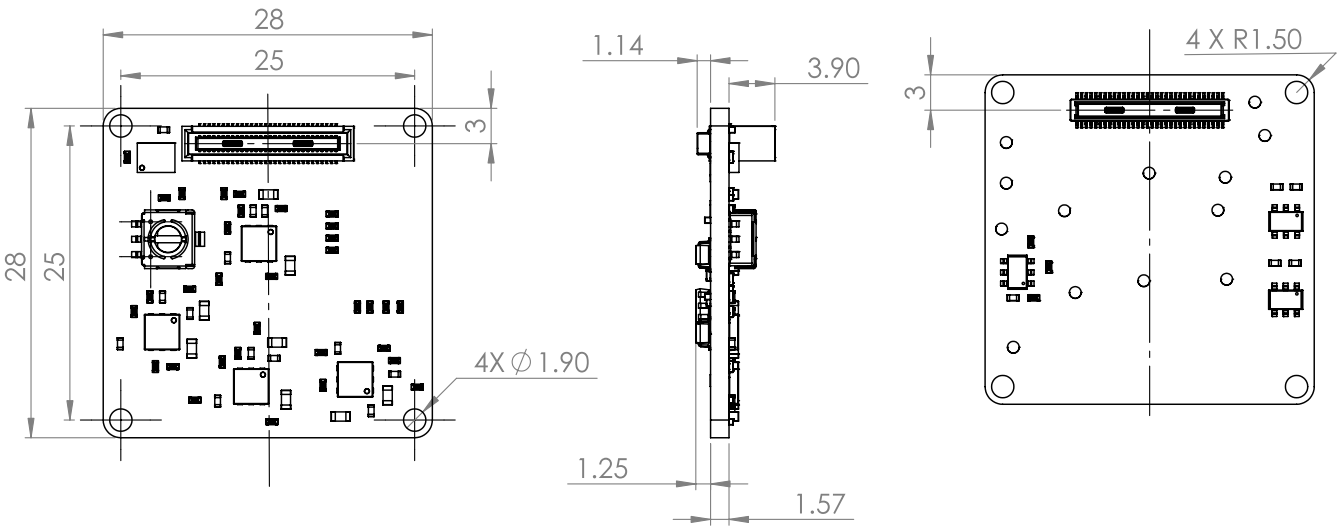


Figure 6: Technical Drawing of FSA-FTx/BC-V1

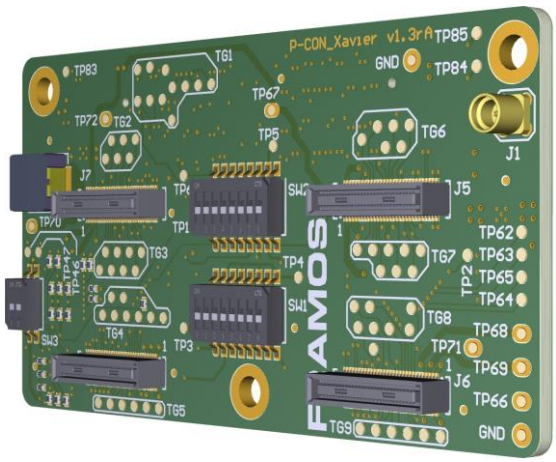
7 FRAMOS Processor Adapter (FPA)

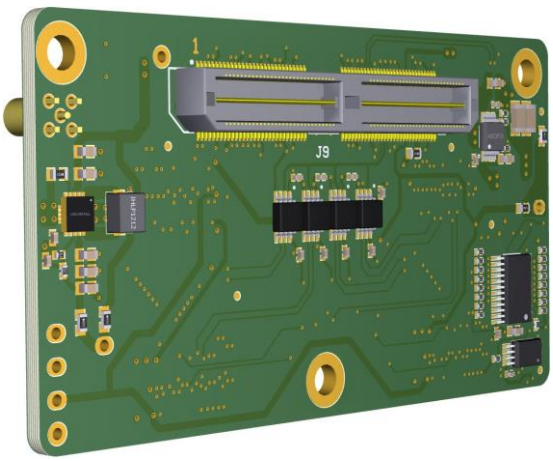
- Connects multiple FSAs to one processor board
- Processor board specific
- Differentiates two input interface types:
  - **A:** MIPI CSI-2
  - **BC:** Sub-LVDS / SLVS (**B**) and SLVS-EC (**C**)

7.1 FPA-4.A/TXA: Quad FPA to NVIDIA Jetson TX2 and AGX Xavier

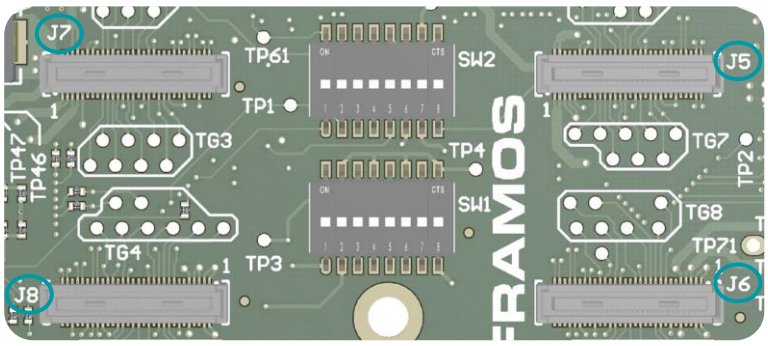
- Four 4-Lane MIPI CSI-2 Inputs
- Signal routing and I2C multiplexing
- Testpoints to important sensor signals
- Dynamic device tree management (EEPROM)
- Configuration of trigger routing

- Compatible Processor Boards:
  - NVIDIA Jetson TX2 Development Kit
  - NVIDIA AGX Xavier Development Kit





7.1.1 J5, J6, J7, J8: Connectors to Sensor Adapters (FSA)



Name	Description	Connector Type	Orientation
J5	Port 1, 4-Lanes CSI-2, to FSA	Hirose DF40HC(4.0)-60DS-0.4V	Pin 1 Printed on PCB next to each connector.
J6	Port 2, 4-Lanes CSI-2, to FSA		
J7	Port 3, 4-Lanes CSI-2 (TX2: 2-Lanes), to FSA		
J8	Port 4, 4-Lanes CSI-2 (TX2: 2-Lanes), to FSA		

Table 10: Image Sensor Connectors on FPA-4.A/TXA-V1

All ports provide the same pinout. The pin assignment is according to the corresponding FSA.

Further notes for signals on FSA connectors J5, J6, J7, J8:

- CAM0_MCLK and CAM1_MCLK are routed through four bus transceiver for better integrity of the signal
- CAM0_PWDN and CAM0_RST signals are routed in parallel to all connectors
- I2C_GP3_CLK and I2C_GP3_DATA are routed parallel to EEPROM and I2C multiplexer (8 channels)
- EEPROM functionality is primarily used to utilize functionality of L4T Plugin manager (driver) but offers additional user space for configuration etc.
- Each FSA connector is connected to two multiplexer channels:
    - MUX-ch0/ch1 are connected to J5
    - MUX-ch2/ch3 are connected to J6
    - MUX-ch4/ch5 are connected to J7
    - MUX-ch6/ch7 are connected to J8

Caution: Direct connection of FSM to FPA (without FSA) or wrong cable orientation will lead to permanent damage of FSM, Adapters or the Processor Board. Using flex cable (FMA-FC-150/60-v1) between FSA and FPA is mandatory.

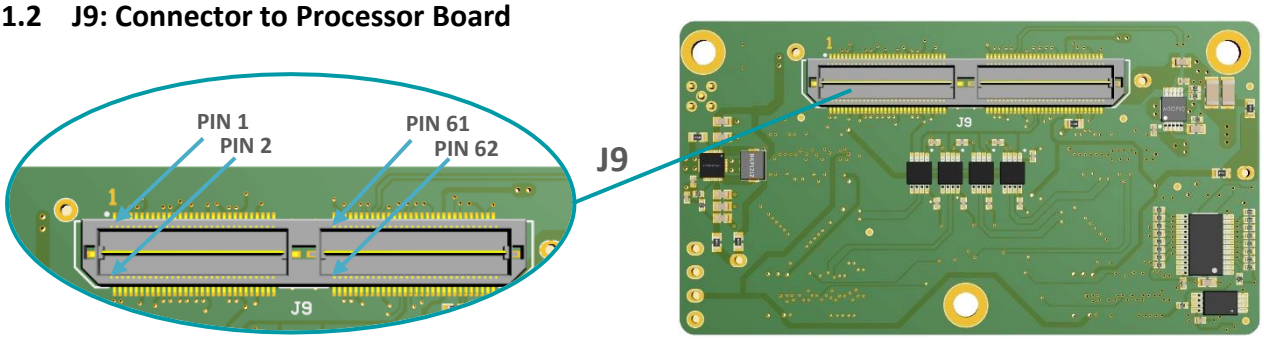
Image Sensor CSI-2 lane Support per Port

The table below shows the possible MIPI CSI-2 lane configurations per FSM / Processor Board combination, that are supported in HW using the FPA-4.A/TXA-V1.

	NVIDIA Jetson TX2				NVIDIA AGX Xavier			
FSM with FSA-FTx/A (all)	**J5**	**J6**	**J7**	**J8**	**J5**	**J6**	**J7**	**J8**
FSM-AR0144	2	2	2	2	2	2	2	2
FSM-AR0521	2 / 4	2 / 4	2	2	2 / 4	2 / 4	2 / 4	2 / 4
FSM-AR1335	2 / 4	2 / 4	2	2	2 / 4	2 / 4	2 / 4	2 / 4
FSM-HDP230	2 / 4	2 / 4	2	2	2 / 4	2 / 4	2 / 4	2 / 4
FSM-IMX264	4	4	-	-	4	4	4	4
FSM-IMX283	4	4	-	-	4	4	4	4
FSM-IMX290	2 / 4	2 / 4	2	2	2 / 4	2 / 4	2 / 4	2 / 4
FSM-IMX296	1	1	1	1	1	1	1	1
FSM-IMX297	1	1	1	1	1	1	1	1
FSM-IMX304	4	4	-	-	4	4	4	4
FSM-IMX327	2 / 4	2 / 4	2	2	2 / 4	2 / 4	2 / 4	2 / 4
FSM-IMX334	4	4	-	-	4	4	4	4
FSM-IMX335	2 / 4	2 / 4	2	2	2 / 4	2 / 4	2 / 4	2 / 4
FSM-IMX412	2 / 4	2 / 4	2	2	2 / 4	2 / 4	2 / 4	2 / 4
FSM-IMX415	2 / 4	2 / 4	2	2	2 / 4	2 / 4	2 / 4	2 / 4
FSM-IMX462	2 / 4	2 / 4	2	2	2 / 4	2 / 4	2 / 4	2 / 4
FSM-IMX464	2 / 4	2 / 4	2	2	2 / 4	2 / 4	2 / 4	2 / 4
FSM-IMX477	2 / 4	2 / 4	2	2	2 / 4	2 / 4	2 / 4	2 / 4
FSM-IMX485	2 / 4	2 / 4	2	2	2 / 4	2 / 4	2 / 4	2 / 4
FSM-IMX530	4	4	-	-	4	4	4	4
FSM-IMX577	2 / 4	2 / 4	2	2	2 / 4	2 / 4	2 / 4	2 / 4

Table 11: Image Sensor Support per Port with FPA-4.A/TXA-V1

7.1.2 J9: Connector to Processor Board



Label: J9

Type: QTH-060-01-L-D-A

Pinout:

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	D_DATA_0_P	2	D_DATA_2_P	61	D_DATA_10_N	62	D_DATA_14_N
3	D_DATA_0_N	4	D_DATA_2_N	63	GND	64	GND
5	GND	6	GND	65	D_CLK_5_P	66	D_CLK_7_P
7	D_CLK_0_P	8	D_CLK_1_P	67	D_CLK_5_N	68	D_CLK_7_N
9	D_CLK_0_N	10	D_CLK_1_N	69	GND	70	GND
11	GND	12	GND	71	D_DATA_11_P	72	D_DATA_15_P
13	D_DATA_1_P	14	D_DATA_3_P	73	D_DATA_11_N	74	D_DATA_15_N
15	D_DATA_1_N	16	D_DATA_3_N	75	I2C_SCL	76	NC
17	GND	18	GND	77	I2C_SDA	78	NC
19	D_DATA_4_P	20	D_DATA_6_P	79	GND	80	GND
21	D_DATA_4_N	22	D_DATA_6_N	81	2V8_AUX	82	2V8_AUX
23	GND	24	GND	83	2V8_AUX	84	NC
25	D_CLK_2_P	26	D_CLK_3_P	85	TP_85	86	XVS0
27	D_CLK_2_N	28	D_CLK_3_N	87	TP_87	88	MCLK_1
29	GND	30	GND	89	TP_89	90	PW_EN_1
31	D_DATA_5_P	32	D_DATA_7_P	91	MCLK_0	92	RST_1
33	D_DATA_5_N	34	D_DATA_7_N	93	PW_EN_0	94	MCLK_2
35	GND	36	GND	95	RST_0	96	NC
37	D_DATA_8_P	38	D_DATA_12_P	97	TP_97	98	NC
39	D_DATA_8_N	40	D_DATA_12_N	99	GND	100	GND
41	GND	42	GND	101	1V2_AUX	102	1V8_AUX
43	D_CLK_4_P	44	D_CLK_6_P	103	TP_103	104	TP_104
45	D_CLK_4_N	46	D_CLK_6_N	105	TP_105	106	TP_106
47	GND	48	GND	107	TP_107	108	3V3_VDD
49	D_DATA_9_P	50	D_DATA_13_P	109	NC	110	3V3_VDD
51	D_DATA_9_N	52	D_DATA_13_N	111	NC	112	TP_112
53	GND	54	GND	113	NC	114	NC
55	NC	56	NC	115	GND	116	GND
57	NC	58	NC	117	TP_117	118	3V3-5V_VDD
59	D_DATA_10_P	60	D_DATA_14_P	119	SYS_PW_EN	120	3V3-5V_VDD

Table 12: Pinout of FPA-4.A/TXA-V1 connector to NVIDIA Jetson TX2 and AGX Xavier

7.1.3 SW1, SW2: Configuration Switches

DIP switches SW1 and SW2 are mainly for interconnecting FSA's triggering signals (XVS, XHS and XTRIG).

DIP switch SW1 is designated to interconnect XVS/XHS pins while DIP switch SW2 is designated to interconnect XTRIG pins and aggregate CAM2_MCLK04(MCLK2) and GPIO25_VDD_SYS_EN(SYS_PW_EN) from FPA in parallel to all FSA connectors.

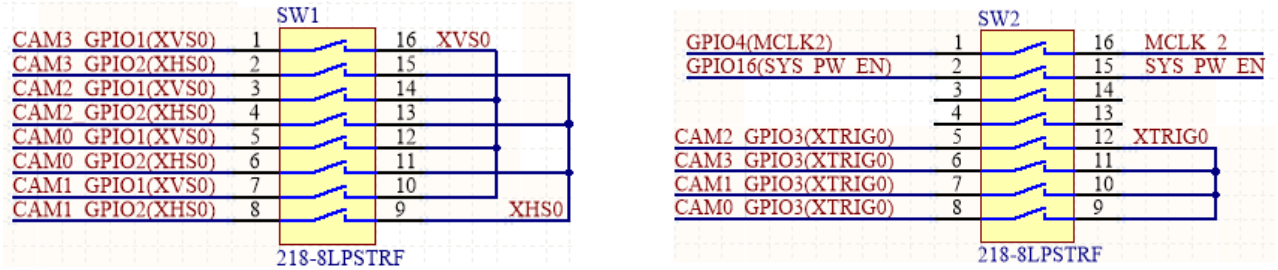


Table 13: Configuration of SW1 and SW2 on FPA-4.A/TXA-V1

7.1.4 SW3: Configuration Switches

DIP switch SW3 is designated to enable/disable FPA EEPROM and it's write protection.

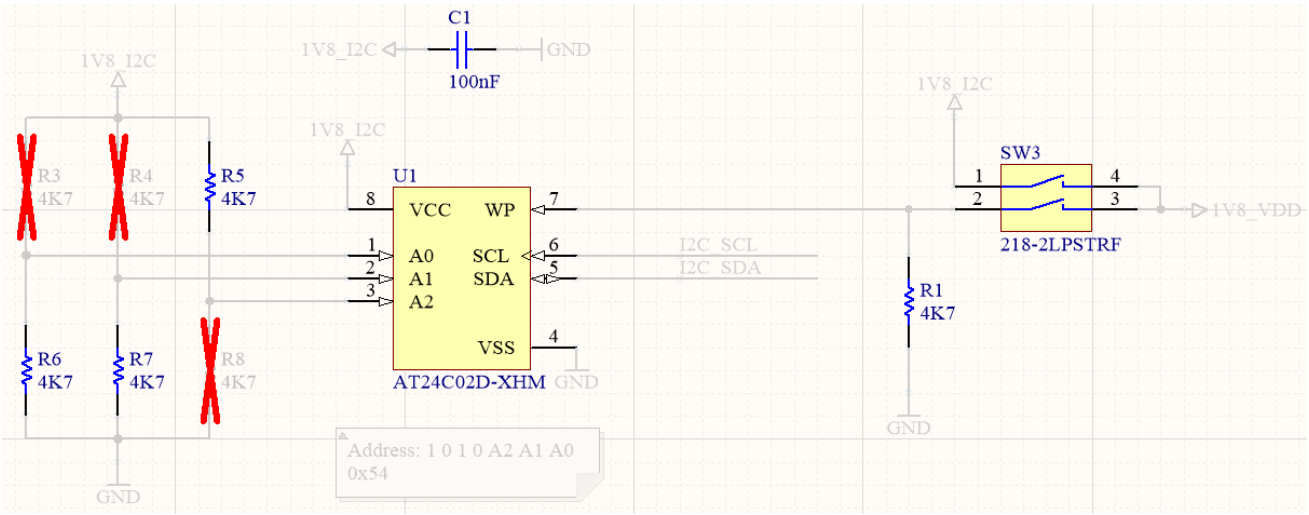
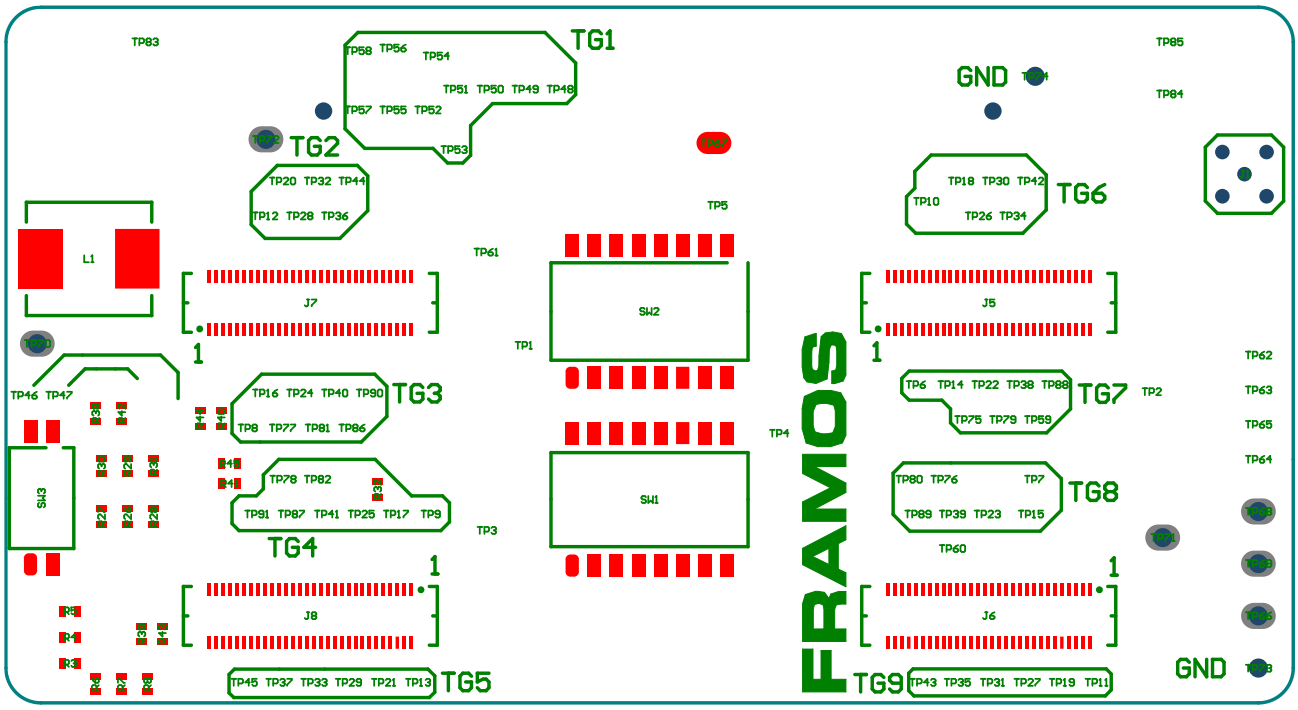


Table 14: Configuration of SW3 on FPA-4.A/TXA-V1

Default state of DIP switches

- SW1 – all positions OFF (XVS/XHS pins are NOT interconnected)
- SW2 – all positions OFF (XTRIG pins are NOT interconnected, MCLK2 and SYS_PW_EN are NOT aggregate)
- SW3 – positions-1 ON, position-2 OFF (EEPROM is ENABLED without write protection)

7.1.5 TGx, TPx: Test Groups and Test Points



Connector J9: TG1 and Ungrouped Test Points

Label	Signal (TG1)	Label	Signal
TP48	TP_85	**TP46**	I2C_SCL
TP49	TP_87	**TP47**	I2C_SDA
TP50	TP_89	**TP61**	MCLK_2
TP51	TP_97	**TP62**	PW_EN_0
TP52	TP_103	**TP63**	PW_EN_1
TP53	TP_104	**TP64**	RST_0
TP54	TP_105	**TP65**	RST_1
TP55	TP_106		
TP56	TP_107		
TP57	TP_112		
TP58	TP_117		

Connector J5 (TG6, TG7) and J6 (TG8, TG9)

Label (J5)	Signal (TG6, TG7)	Label (J6)	Signal (TG8, TG9)
TP59	CAM0_MCLK_0	**TP60**	CAM1_MCLK_0
TP88	CAM0_MCLK_1	**TP89**	CAM1_MCLK_1
TP6	CAM0_GPIO14	**TP7**	CAM1_GPIO14
TP10	CAM0_GPIO15(SPI_MISO)	**TP11**	CAM1_GPIO15(SPI_MISO)
TP14	CAM0_GPIO0(XMASTER0)	**TP15**	CAM1_GPIO0(XMASTER0)
TP18	CAM0_GPIO8	**TP19**	CAM1_GPIO8
TP22	CAM0_GPIO17(SPI_CS)	**TP23**	CAM1_GPIO17(SPI_CS)
TP26	CAM0_GPIO9	**TP27**	CAM1_GPIO9
TP30	CAM0_GPIO10	**TP31**	CAM1_GPIO10
TP34	CAM0_GPIO11	**TP35**	CAM1_GPIO11
TP38	CAM0_GPIO6	**TP39**	CAM1_GPIO6
TP42	CAM0_GPIO7	**TP43**	CAM1_GPIO7
TP75	I2C_0_SCL(SPI_SCK)	**TP76**	I2C_2_SCL(SPI_SCK)
TP79	I2C_0_SDA(SPI_MOSI)	**TP80**	I2C_2_SDA(SPI_MOSI)

Version v1.1b from 2020-10-01

Connector J7 (TG2, TG3) and J8 (TG4, TG5)

Label (J5)	Signal (TG6, TG7)	Label (J6)	Signal (TG8, TG9)
TP86	CAM2_MCLK_0	**TP87**	CAM3_MCLK_0
TP90	CAM2_MCLK_1	**TP91**	CAM3_MCLK_1
TP8	CAM2_GPIO14	**TP9**	CAM3_GPIO14
TP12	CAM2_GPIO15(SPI_MISO)	**TP13**	CAM3_GPIO15(SPI_MISO)
TP16	CAM2_GPIO0(XMASTER0)	**TP17**	CAM3_GPIO0(XMASTER0)
TP20	CAM2_GPIO8	**TP21**	CAM3_GPIO8
TP24	CAM2_GPIO17(SPI_CS)	**TP25**	CAM3_GPIO17(SPI_CS)
TP28	CAM2_GPIO9	**TP29**	CAM3_GPIO9
TP32	CAM2_GPIO10	**TP33**	CAM3_GPIO10
TP36	CAM2_GPIO11	**TP37**	CAM3_GPIO11
TP40	CAM2_GPIO6	**TP41**	CAM3_GPIO6
TP44	CAM2_GPIO7	**TP45**	CAM3_GPIO7
TP77	I2C_4_SCL(SPI_SCK)	**TP78**	I2C_6_SCL(SPI_SCK)
TP81	I2C_4_SDA(SPI_MOSI)	**TP82**	I2C_6_SDA(SPI_MOSI)

Other Test Points (Ungrouped)

Label	Signal
TP1	GPIO16(SYS_PW_EN)
TP2	GPIO5(MCLK3)
TP3	XVS0
TP4	XHS0
TP74	GND
TP5	XTRIG0
TP83	GPIO4(MCLK2)
TP84	CAM0_GPIO2(XHS0)
TP85	CAM0_GPIO3(XTRIG0)

7.1.6 Technical Drawing

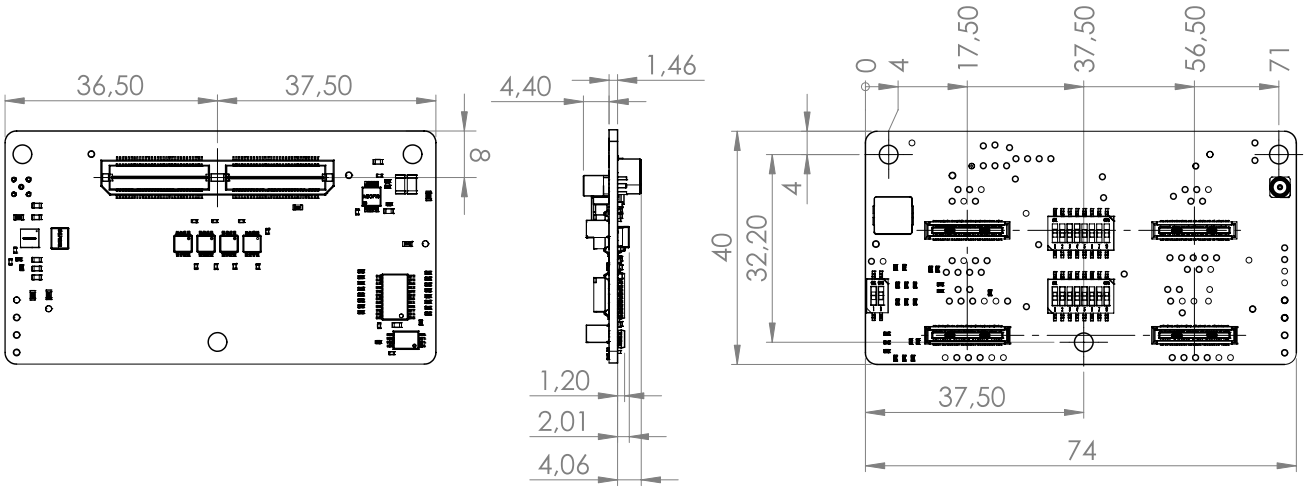
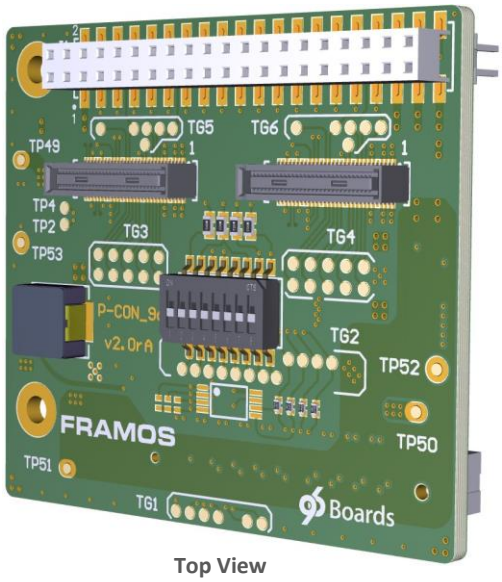


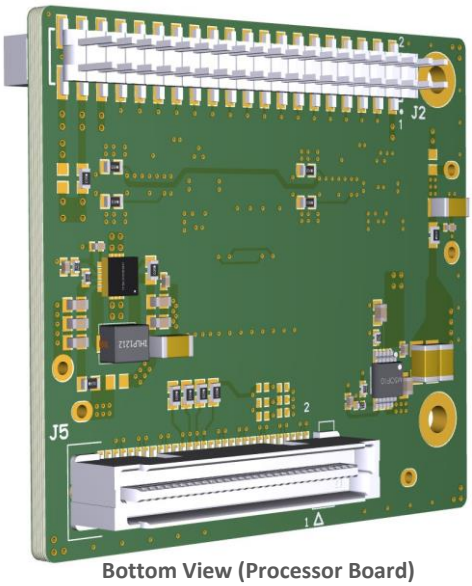
Figure 7: Technical Drawing of FPA-4.A/TXA-V1

7.2 FPA-2.A/96B: Dual FPA to 96Boards.org Consumer Edition

- Two MIPI CSI-2 Inputs with 4- and 2-Lanes
- Signal routing and I2C multiplexing
- EEPROM for dynamic device tree management
- Testpoints to important sensor signals
- Configuration of trigger routing
- Compatible Processor Boards:
  - 96boards Consumer Edition (CE) Standard https://www.96boards.org/products/ce/

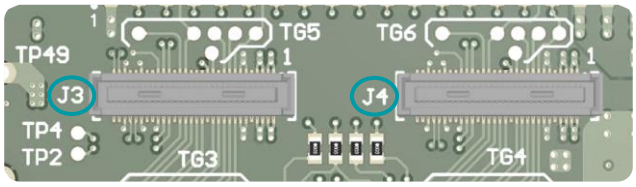


Top View



Bottom View (Processor Board)

7.2.1.1 J3, J4: Image Sensor Connectors



Name	Description	Connector Type	Orientation
J3	Port 1, 4-Lanes CSI-2, to FSA	Hirose DF40HC(4.0)-60DS-0.4V	Pin 1 Printed on PCB next to each connector.
J4	Port 2, 4-Lanes CSI-2, to FSA[2]		

Table 15: Image Sensor Connectors on FPA-2.A/A-V1

All ports provide the same pinout. The pin assignment is according to the corresponding FSA.

Caution: Direct connection of FSM to FPA (without FSA) or wrong cable orientation will lead to permanent damage of FSM, Adapters or the Processor Board. Using flex cable (FMA-FC-150/60-v1) between FSA and FPA is mandatory.

[2] The usage of the second port might require a minor hardware modification by the user. Further details are described in the “User Guide” in the platform specific software package.

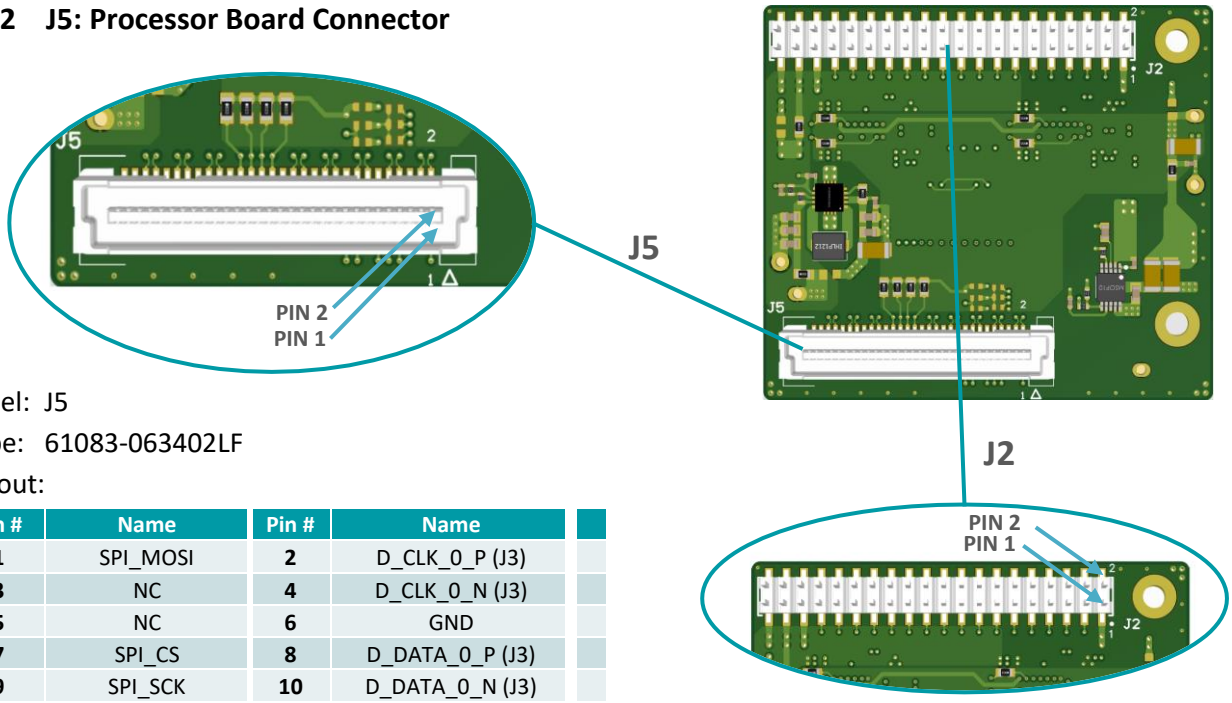
Image Sensor Support per Port

The table below shows the possible MIPI CSI-2 lane configurations per FSM / Processor Board combination, that are supported in HW using the FPA-2.A/96B-V1.

	96Boards CE	
FSM with FSA-FTx/A (all)	**J5**	**J6**
FSM-AR0144	2	2
FSM-AR0521	2 / 4	2
FSM-AR1335	2 / 4	2
FSM-HDP230	4	2
FSM-IMX264	4	-
FSM-IMX283	4	-
FSM-IMX290	2 / 4	2
FSM-IMX296	1	1
FSM-IMX297	1	1
FSM-IMX304	4	-
FSM-IMX327	2 / 4	2
FSM-IMX334	4	-
FSM-IMX335	2 / 4	2
FSM-IMX412	2 / 4	2
FSM-IMX415	2 / 4	2
FSM-IMX462	2 / 4	2
FSM-IMX464	2 / 4	2
FSM-IMX477	2 / 4	2
FSM-IMX485	2 / 4	2
FSM-IMX530	4	-
FSM-IMX577	2 / 4	2

Table 16: Image Sensor Support per Port with FPA-2.A/96B-V1

7.2.2 J5: Processor Board Connector



Label: J5
Type: 61083-063402LF
Pinout:

Pin #	Name	Pin #	Name
1	SPI_MOSI	2	D_CLK_0_P (J3)
3	NC	4	D_CLK_0_N (J3)
5	NC	6	GND
7	SPI_CS	8	D_DATA_0_P (J3)
9	SPI_SCK	10	D_DATA_0_N (J3)
11	SPI_MISO	12	GND
13	GND	14	D_DATA_1_P (J3)
15	MCLK_0	16	D_DATA_1_N (J3)
17	MCLK_1	18	GND
19	GND	20	D_DATA_2_P (J3)
21	NC	22	D_DATA_2_N (J3)
23	NC	24	GND
25	GND	26	D_DATA_3_P (J3)
27	NC	28	D_DATA_3_N (J3)
29	NC	30	GND
31	GND	32	I2C_0_SCL
33	NC	34	I2C_0_SDA
35	NC	36	I2C_2_SCL
37	GND	38	I2C_2_SDA
39	NC	40	GND
41	NC	42	D_DATA_4_P (J4)
43	GND	44	D_DATA_4_N (J4)
45	NC	46	GND
47	NC	48	D_DATA_5_P (J4)
49	GND	50	D_DATA_5_N (J4)
51	NC	52	GND
53	NC	54	D_CLK_0_P (J4)
55	GND	56	D_CLK_0_N (J4)
57	NC	58	GND
59	NC	60	NC

Label: J1/J2
Type: 61083-063402LF
Pinout:

Pin #	Name	Pin #	Name
1	GND	2	GND
3	96B_UART0_CTS	4	96B_PWR_BTNn
5	96B_UART0_TXD	6	96B_PWR_BTNn
7	96B_UART0_RXD	8	96B_SPI0_CLK
9	96B_UART0_RTS	10	96B_SPI0_MISO
11	96B_UART1_TXD	12	96B_SPI0_CS
13	96B_UART1_RXD	14	96B_SPI0_MOSI
15	96B_SCL_0	16	96B_PCM_FS
17	96B_SDA_0	18	96B_PCM_CLK
19	96B_SCL_1	20	96B_PCM_DO
21	96B_SDA_1	22	96B_PCM_DI
23	96B_GPIO_A	24	96B_GPIO_B
25	96B_GPIO_C	26	96B_GPIO_D
27	96B_GPIO_E	28	96B_GPIO_F
29	96B_GPIO_G	30	96B_GPIO_H
31	CAM0_RST_0	32	CAM0_PW_EN_0
33	CAM1_RST_0	34	CAM1_PW_EN_0
35	96B_1V8	36	96B_SYS_DCIN
37	96B_5V0	38	
39	GND	40	GND

Table 17: Pinout of FPA-2.A/96B-V1 connector to 96Boards.org Consumer Edition Standard

7.2.3 SW1: Configuration Switch

The DIP switch SW1 is for interconnecting FSA's triggering signals (XVS, XHS and XTRIG). It is designated to interconnect XVS, XHS and XTRIG pins from FPA in parallel to both FSA connectors.

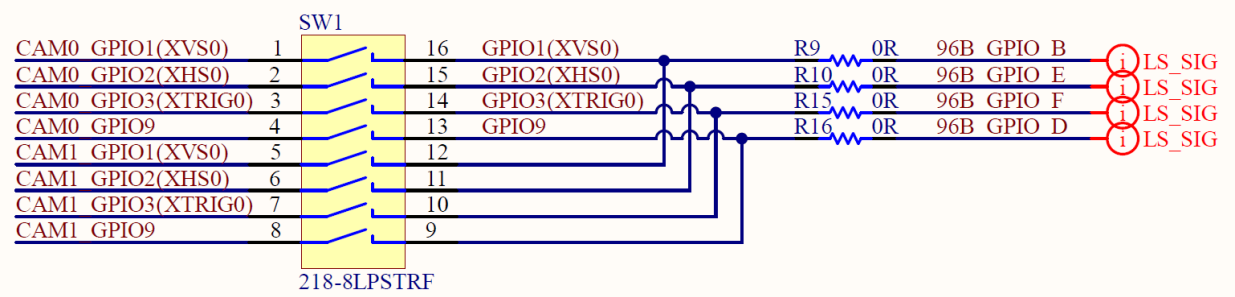


Table 18: Configuration of SW1 on FPA-2.A/96B-V1

Default state of DIP switch

- SW1 – all positions OFF (XVS/XHS pins are NOT interconnected)

7.2.4 TGx, TPx: Test Groups and Test Points

7.2.5 Ungrouped (according to silk print)

Label	Signal	Label	Signal
TP2	GPIO4(MCLK2)	**TP51**	5V0_VDD
TP4	GPIO5(MCLK3)	**TP52**	GND
TP49	1V8_VDD	**TP53**	GND
TP50	3V8_VDD		

TG1: Clocks and SPI

Label	Signal	Label	Signal
TP1	MCLK_0	**TP55**	SPI_CS
TP3	MCLK_1	**TP56**	SPI_SCK
TP54	SPI_MOSI	**TP57**	SPI_MISO

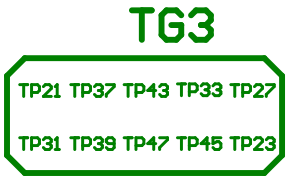
TG2: Synchronisation Signals

Label	Signal	Label	Signal
TP9	CAM0_I2C_0_SCL(SPI_SCK)	**TP18**	CAM1_GPIO3(XTRIG0)
TP10	CAM1_I2C_0_SCL(SPI_SCK)	**TP35**	CAM0_GPIO9
TP11	CAM0_I2C_0_SDA(SPI_MOSI)	**TP36**	CAM1_GPIO9
TP12	CAM1_I2C_0_SDA(SPI_MOSI)		
TP13	CAM0_GPIO1(XVS0)		
TP14	CAM1_GPIO1(XVS0)		
TP15	CAM0_GPIO2(XHS0)		
TP16	CAM1_GPIO2(XHS0)		
TP17	CAM0_GPIO3(XTRIG0)		

Version v1.1b from 2020-10-01

TG3: Control Signals and GPIOs J3 (CAM0)

Label	Signal	Label	Signal
TP21	CAM0_PW_EN_1	TP37	CAM0_GPIO10
TP23	CAM0_GPIO15(SPI_MISO)	TP39	CAM0_GPIO11
TP27	CAM0_RST_1	TP43	CAM0_GPIO16(SYS_PW_EN)
TP31	CAM0_GPIO7	TP45	CAM0_I2C_1_SCL
TP33	CAM0_GPIO8	TP47	CAM0_I2C_1_SDA



TG4: Control Signals and GPIOs J4 (CAM1)

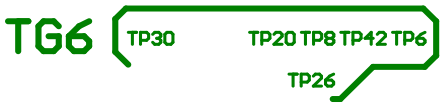
Label	Signal	Label	Signal
TP22	CAM1_PW_EN_1	TP38	CAM1_GPIO10
TP24	CAM1_GPIO15(SPI_MISO)	TP40	CAM1_GPIO11
TP28	CAM1_RST_1	TP44	CAM1_GPIO16(SYS_PW_EN)
TP32	CAM1_GPIO7	TP46	CAM1_I2C_1_SCL
TP34	CAM1_GPIO8	TP48	CAM1_I2C_1_SDA

TG6: Control Signals and GPIOs J3 (CAM0)

Label	Signal	Label	Signal
TP5	CAM0_RST_0	TP25	CAM0_GPIO17(SPI_CS)
TP7	CAM0_GPIO0(XMASTER0)	TP29	CAM0_GPIO6
TP19	CAM0_PW_EN_0	TP41	CAM0_GPIO14

TG6: Control Signals and GPIOs J4 (CAM1)

Label	Signal	Label	Signal
TP6	CAM1_RST_0	TP26	CAM1_GPIO17(SPI_CS)
TP8	CAM1_GPIO0(XMASTER0)	TP30	CAM1_GPIO6
TP20	CAM1_PW_EN_0	TP42	CAM1_GPIO14



7.2.6 Technical Drawing

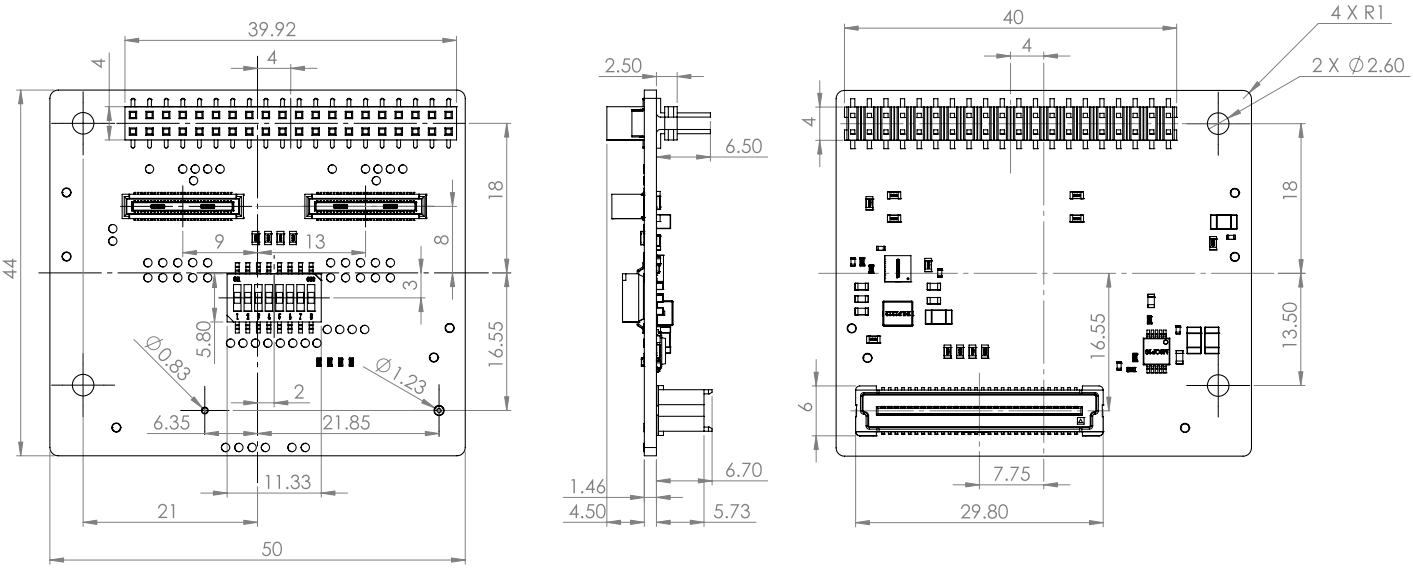
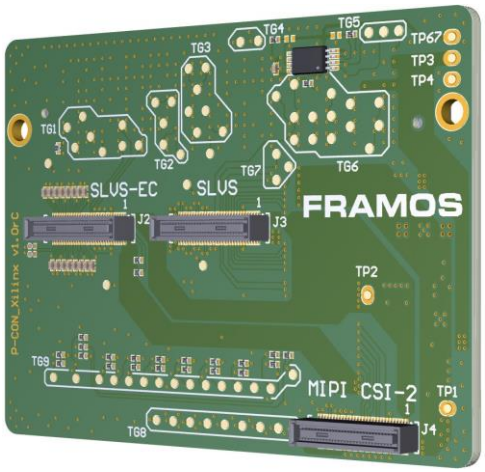
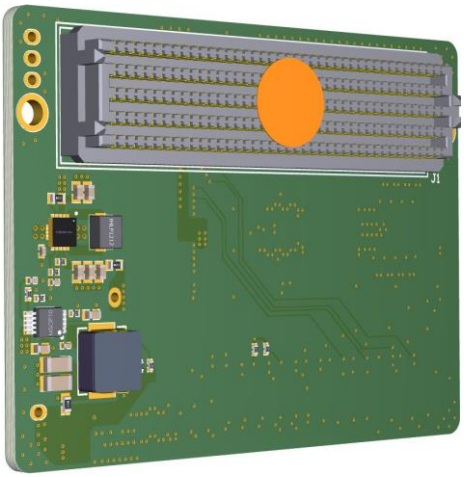


Figure 8: Technical Drawing of FPA-2.A/96B-V1

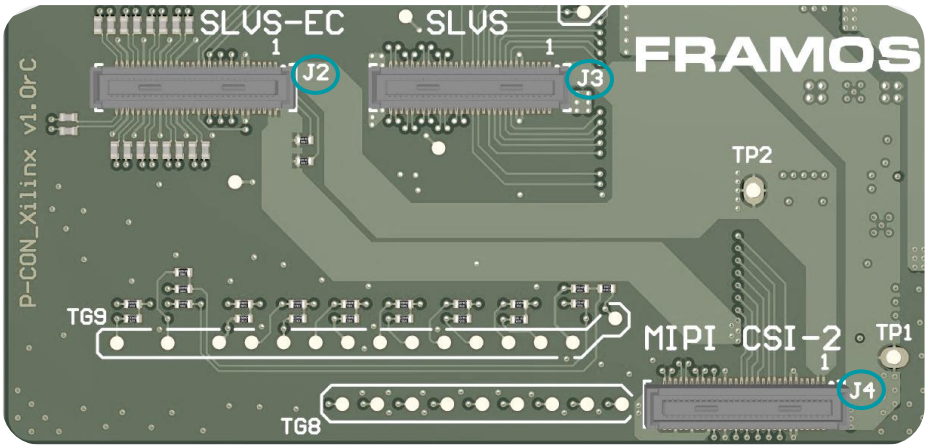
7.3 FPA-ABC/XX1: Multi-Format FPA to Xilinx Development Boards

- Three inputs, one for each interface:
  - SLVS-EC
  - Sub-LVDS / SLVS
  - MIPI CSI-2
- EEPROM for dynamic device tree management
- Testpoints to important sensor signals
- Configurable trigger routing
- Compatible Processor Boards:
  - Various Xilinx Development Boards





7.3.1 Image Sensor Connectors



Label	Name	Description	Connector Type	FPGA Routing
J2	SLVS-EC	Port 2, 8-Lanes SLVS-EC, to FSA	Hirose DF40HC(4.0)-60DS-0.4V	8-Lanes to Transceivers
J3	SLVS	Port 1, 8-Lanes SLVS / Sub-LVDS, to FSA		8-Lanes to differential IOs
J4	MIPI CSI-2	Port 3, 4-Lanes MIPI CSI-2, to FSA		4-Lanes to CSI-2 D-PHY

Table 19: Image Sensor Connectors on FPA-ABC/XX1-V1

All ports provide the same pinout. The pin assignment is according to the corresponding FSA.

Caution: Direct connection of FSM to FPA (without FSA) or wrong cable orientation will lead to permanent damage of FSM, Adapters or the Processor Board. Using flex cable (FMA-FC-150/60-v1) between FSA and FPA is mandatory.

Processor Board Compatibility Matrix

The FPA has been designed to comply to the following Xilinx Development Boards.

Xilinx Development Board	SLVS-EC	SLVS	MIPI CSI-2
AC701-G (Artix-7)	Yes	TBD	TBD
KC705-G (Kintex-7)	Yes	TBD	TBD
ZC706-G (Zynq-7000)	Yes	TBD	TBD
KCU105-G (Kintex UltraScale)	Yes	Yes	TBD
KCU116-G (Kintex UltraScale+)	Yes	TBD	TBD
ZCU102-G (Zynq UltraScale+)	Yes	Yes	Yes

Note – SLVS-EC: The different Xilinx Development Boards provide access to a different count of Gigabit Transceivers (GTx). This might limit the utilization of the 8-Lanes available from the FPA. Please refer to the datasheet of the Xilinx Development Board for more information.

Note - MIPI CSI-2: The Xilinx XCU102-G provides hard D-PHY lanes on the appropriate pins of the FPA connector. The usage of the MIPI CSI-2 port is routed but has not been verified. Operation is in the responsibility of the user. Further Xilinx Development Kits might be compatible but have not been validated for correct electrical connectivity.

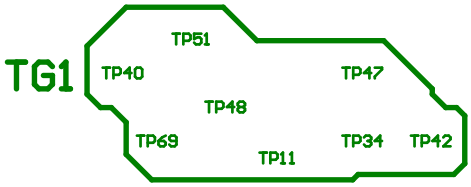
7.3.2 TGx, TPx: Test Groups and Test Points

Ungrouped (according to silk print)

Label	Signal	Label	Signal
TP1	1V8_VDD	**TP67**	UTIL_3V3_10A
TP2	3V8_VDD	**TP75**	GND
TP3	UTIL_3V3	**TP76**	GND
TP4	GND	**TP77**	GND
TP12	CAM1_GPIO0(XMASTER0)	**TP78**	GND

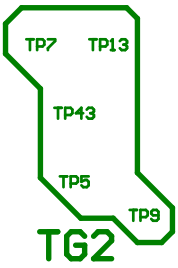
TG1: Clocks and various GPIOs

Label	Signal	Label	Signal
TP11	CAM1_GPIO8(TOUT1)	**TP47**	CAM1_GPIO14
TP34	CAM1_GPIO10	**TP48**	CAM1_MCLK0
TP40	CAM2_GPIO3(XTRIG0)	**TP51**	CAM3_MCLK0
TP42	CAM1_GPIO16	**TP69**	CAM2_MCLK0



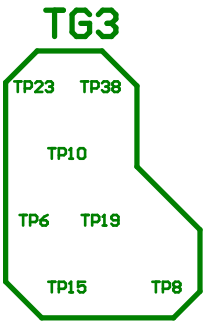
TG2: Various

Label	Signal	Label	Signal
TP5	CAM1_I2C_0_SDA(SPI_MOSI)	**TP13**	CAM1_GPIO9(TOUT2)
TP7	CAM1_GPIO15(SPI_MISO)	**TP43**	CAM1_RST0
TP9	CAM1_GPIO11(TOUT0)		



TG3:

Label	Signal	Label	Signal
TP6	CAM1_I2C_0_SCL(SPI_SCK)	**TP19**	CAM1_GPIO3(XTRIG0)
TP8	CAM1_GPIO17(SPI_CS)	**TP23**	CAM1_GPIO2(XHS0)
TP10	CAM1_GPIO6(SLAMODE)	**TP38**	CAM1_GPIO1(XVS0)
TP15	CAM1_GPIO7(XTRIG2)		



TG4: I2C Clock and Data

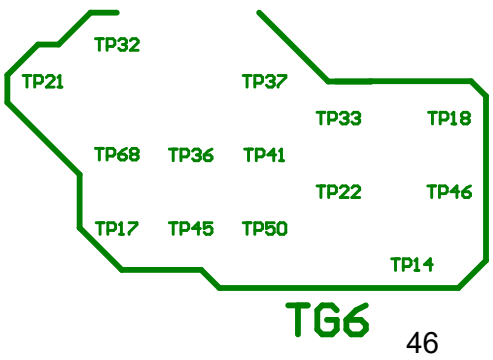
Label	Signal
TP25	SCL
TP26	SDA

TG5: EEPROM Address

Label	Signal
TP27	GA1
TP28	GA0
TP30	GND

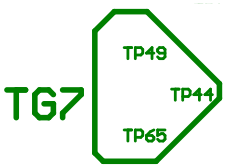
TG6:

Label	Signal	Label	Signal
TP14	CAM3_RST0	**TP36**	CAM2_GPIO7(XTRIG2)
TP17	CAM2_GPIO6(SLAMODE)	**TP37**	CAM3_I2C_0_SDA(SPI_MOSI)
TP18	CAM3_GPIO0(XMASTER0)	**TP41**	CAM3_GPIO2(XHS0)
TP21	CAM2_GPIO8(TOUT1)	**TP45**	CAM2_GPIO2(XHS0)
TP22	CAM3_I2C_0_SCL(SPI_SCK)	**TP46**	CAM3_GPIO3(XTRIG0)
TP32	CAM2_GPIO0(XMASTER0)	**TP50**	CAM2_GPIO1(XVS0)
TP33	CAM3_GPIO1(XVS0)	**TP68**	CAM2_RST0



TG7:

Label	Signal
TP44	CAM2_GPIO9(TOUT2)
TP49	CAM2_GPIO10
TP64	CAM3_GPIO5(MCLK3)



TG8:

Label	Signal
TP52	CAM3_GPIO16(SYS_PW_EN)
TP53	CAM3_GPIO8
TP54	CAM3_GPIO14
TP55	CAM3_RST1
TP60	CAM3_GPIO6
TP61	CAM3_GPIO7

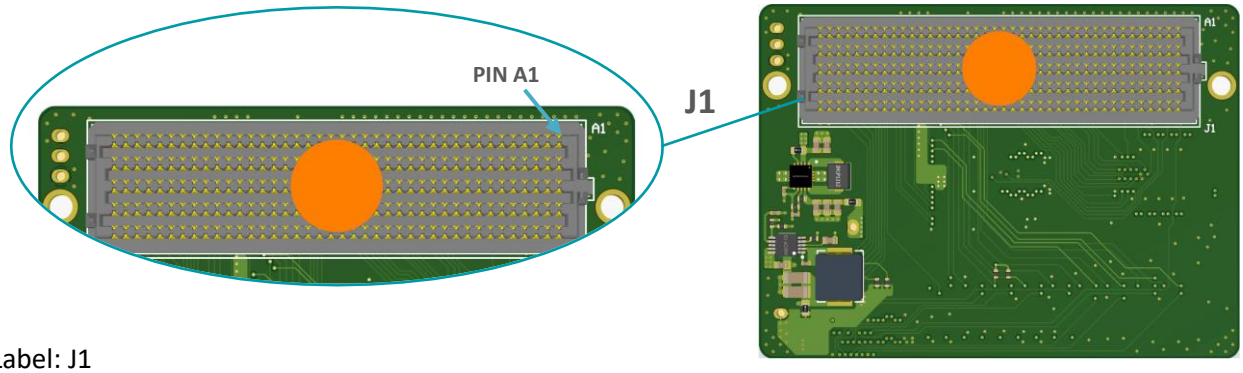
Label	Signal
TP62	CAM3_GPIO4(MCLK2)
TP63	CAM3_MCLK1
TP64	CAM3_GPIO5(MCLK3)

TG9:

Label	Signal
TP16	CAM2_I2C_0_SDA(SPI_MOSI)
TP20	CAM2_I2C_0_SCL(SPI_SCK)
TP24	CAM2_GPIO15(SPI_MISO)
TP35	CAM2_GPIO17(SPI_CS)
TP39	CAM2_GPIO11(TOUT0)
TP56	CAM3_GPIO15(SPI_MISO)
TP57	CAM3_I2C_1_SCL
TP58	CAM3_GPIO17(SPI_CS)

Label	Signal
TP59	CAM3_GPIO9
TP66	CAM2_GPIO14
TP70	CAM3_I2C_1_SDA
TP71	CAM3_GPIO10
TP72	CAM3_GPIO11
TP73	CAM3_PW_EN0
TP74	CAM3_PW_EN1

7.3.3 Processor Board Connector



Label: J1
Type: ASP-134488-01
Pinout (A – J): Table 20 / Table 21
Notes: **CAM1**: J2 (SLVS-EC), **CAM2**: J3 (SLVS), **CAM3**: J4 (MIPI CSI-2)

Table 20: Pinout J1 - Part1 (A-E) of FPA-ABC/XX1-V1 connector to Xilinx Development Board

PIN #	A	B	C	D	E
1	GND	NC	GND	NC	GND
2	FMC_CAM1_DO1_P	GND	NC	GND	NC
3	FMC_CAM1_DO1_N	GND	NC	GND	NC
4	GND	NC	GND	FMC_CAM1_D_CLK_0_P	GND
5	GND	NC	GND	FMC_CAM1_D_CLK_0_N	GND
6	FMC_CAM1_DO2_P	GND	FMC_CAM1_DO0_P	GND	NC
7	FMC_CAM1_DO2_N	GND	FMC_CAM1_DO0_N	GND	NC
8	GND	NC	GND	CAM2_D_DATA_1_P	GND
9	GND	NC	GND	CAM2_D_DATA_1_N	NC
10	FMC_CAM1_DO3_P	GND	CAM2_D_DATA_5_P	GND	NC
11	FMC_CAM1_DO3_N	GND	CAM2_D_DATA_5_N	CAM2_D_DATA_6_P	GND
12	GND	FMC_CAM1_DO7_P	GND	CAM2_D_DATA_6_N	NC
13	GND	FMC_CAM1_DO7_N	GND	GND	NC
14	FMC_CAM1_DO4_P	GND	CAM2_D_DATA_7_P	CAM1_GPIO15(SPI_MISO)	GND
15	FMC_CAM1_DO4_N	GND	CAM2_D_DATA_7_N	CAM1_GPIO9(TOUT2)	NC
16	GND	FMC_CAM1_DO6_P	GND	GND	NC
17	GND	FMC_CAM1_DO6_N	GND	CAM1_GPIO2(XHS0)	GND
18	FMC_CAM1_DO5_P	GND	CAM1_GPIO1(XVS0)	CAM1_GPIO6(SLAMODE)	NC
19	FMC_CAM1_DO5_N	GND	CAM_GPIO14	GND	NC
20	GND	NC	GND	CAM_GPIO10	GND
21	GND	NC	GND	CAM_GPIO9	NC
22	NC	GND	CAM_GPIO11	GND	NC
23	NC	GND	CAM_GPIO15	CAM3_D_CLK_0_P	GND
24	GND	NC	GND	CAM3_D_CLK_0_N	NC
25	GND	NC	GND	GND	NC
26	NC	GND	CAM_I2C_SDA	CAM3_D_DATA_3_P	GND
27	NC	GND	CAM_GPIO17	CAM3_D_DATA_3_N	NC
28	GND	NC	GND	GND	NC
29	GND	NC	GND	NC	GND
30	NC	GND	SCL	TDI	NC
31	NC	GND	SDA	TDO	NC
32	GND	NC	GND	UTIL_3V3_10A	GND
33	GND	NC	GND	NC	NC
34	NC	GND	GA0	NC	NC
35	NC	GND	NC	GA1	GND
36	GND	NC	NC	UTIL_3V3	NC
37	GND	NC	NC	GND	NC
38	NC	GND	NC	UTIL_3V3	GND
39	NC	GND	UTIL_3V3	GND	VADJ
40	GND	NC	NC	UTIL_3V3	GND

Table 21: Pinout J1 – Part2 (F-J) of FPA-ABC/XX1-V1 connector to Xilinx Development Board

PIN #	F	G	H	I	J
1	NC	GND	NC	GND	NC
2	GND	CAM2_GPIO3(XTRIG)	PRSNT_M2C_L	NC	GND
3	GND	CAM3_MCLK0	GND	NC	GND
4	NC	GND	CAM2_MCLK_0	GND	NC
5	NC	GND	CAM1_MCLK_0	GND	NC
6	GND	CAM2_D_CLK_0_P	GND	NC	GND
7	NC	CAM2_D_CLK_0_N	CAM1_GPIO8(TOUT1)	NC	NC
8	NC	GND	CAM1_GPIO10	GND	NC
9	GND	CAM2_D_DATA_3_P	GND	NC	GND
10	NC	CAM2_D_DATA_3_N	CAM2_D_DATA_0_P	NC	NC
11	NC	GND	CAM2_D_DATA_0_N	GND	NC
12	GND	CAM2_D_DATA_4_P	GND	NC	GND
13	NC	CAM2_D_DATA_4_N	CAM2_D_DATA_2_P	NC	NC
14	NC	GND	CAM2_D_DATA_2_N	GND	NC
15	GND	CAM1_RST0	GND	NC	GND
16	NC	CAM1_I2C_0_SDA(SPI_MOSI)	CAM1_GPIO11(TOUT0)	NC	NC
17	NC	GND	CAM1_GPIO7(XTRIG2)	GND	NC
18	GND	CAM1_I2C_0_SCL(SPI_SCK)	GND	NC	GND
19	NC	CAM1_GPIO3(XTRIG0)	CAM1_GPIO0(XMASTER0)	NC	NC
20	NC	GND	CAM1_GPIO17(SPI_CS)	GND	NC
21	GND	CAM3_D_CLK_1_P	GND	NC	GND
22	NC	CAM3_D_CLK_1_N	CAM3_D_DATA_2_P	NC	NC
23	NC	GND	CAM3_D_DATA_2_N	GND	NC
24	GND	CAM3_D_DATA_0_P	GND	NC	GND
25	NC	CAM3_D_DATA_0_N	CAM3_D_DATA_1_P	NC	NC
26	NC	GND	CAM3_D_DATA_1_N	GND	NC
27	GND	CAM_I2C_SCL	GND	NC	GND
28	NC	CAM2_GPIO8(TOUT1)	CAM2_RST0	NC	NC
29	NC	GND	CAM2_GPIO6(SLAMODE)	GND	NC
30	GND	CAM2_GPIO0(XMASTER0)	GND	NC	GND
31	NC	CAM2_GPIO7(XTRIG2)	CAM2_GPIO2(XHS0)	NC	NC
32	NC	GND	CAM2_GPIO1(XVS0)	GND	NC
33	GND	CAM3_I2C_0_SDA(SPI_MOSI)	GND	NC	GND
34	NC	CAM3_GPIO2(XHS0)	CAM_GPIO16	NC	NC
35	NC	GND	CAM3_I2C_0_SCL(SPI_SCK)	GND	NC
36	GND	CAM3_GPIO1(XVS0)	GND	NC	GND
37	NC	CAM3_GPIO0(XMASTER0)	CAM3_RST0	NC	NC
38	NC	GND	CAM3_GPIO3(XTRIG0)	GND	NC
39	GND	NC	GND	NC	GND
40	NC	GND	NC	GND	NC

7.3.4 Technical Drawing

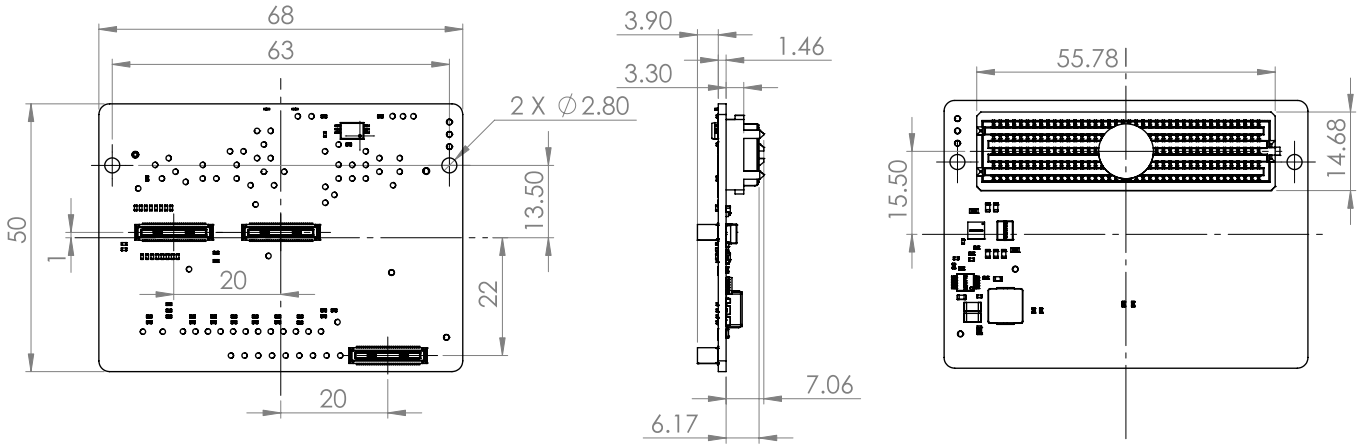


Figure 9: Technical Drawing of FPA-4.A/TXA-V1

8 FRAMOS Module Accessories (FMA)

8.1 FMA-MNT-CCS/280_v1: C/CS-Mount for 28mm Footprint

CS-mount body delivered with 5mm CS- to C-Mount extension ring.

- Material: AlMgSi0.5
- Finish: Black Anodizing

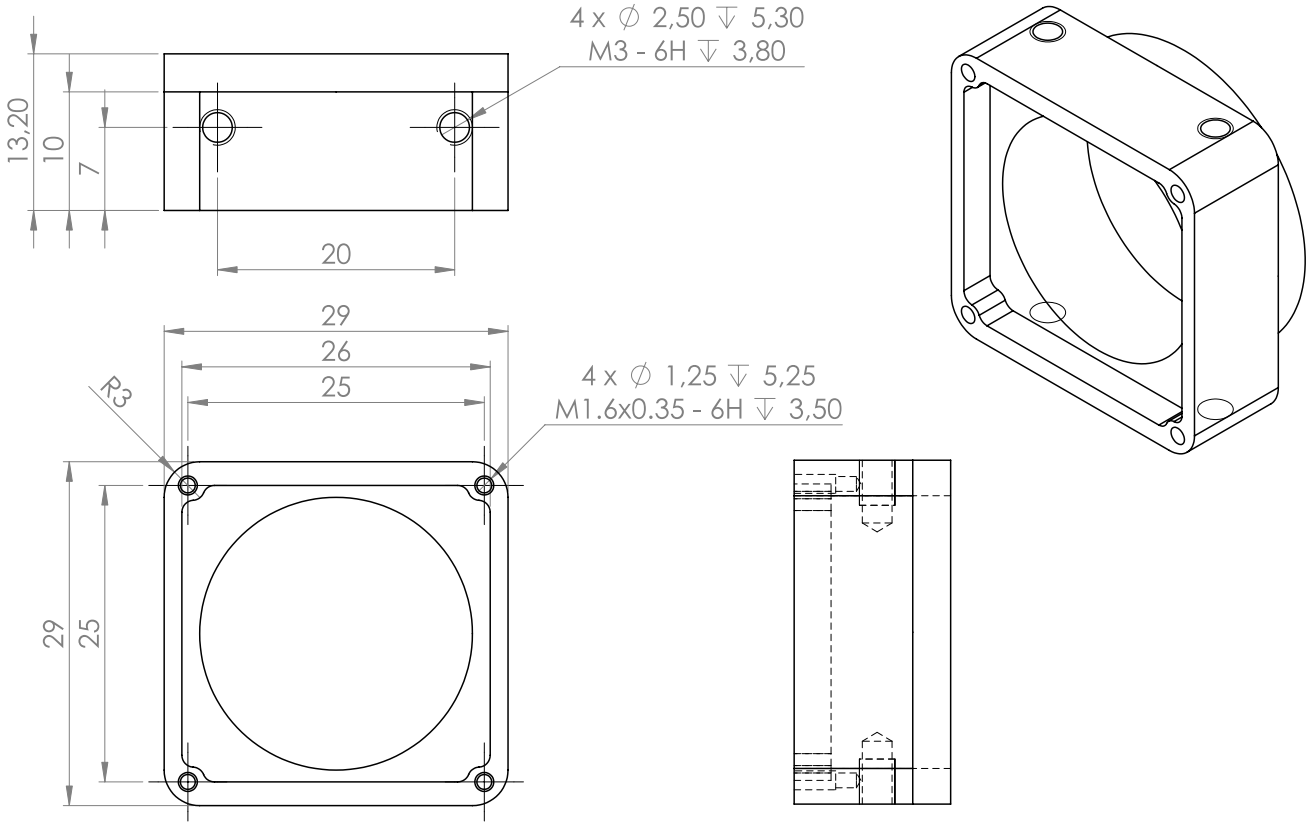


Figure 10: CS-Mount Body for 28 mm FSM

Note: The actual distance of the active sensor surface to PCB and different types of sensor cover glasses on the different supported sensors might require the adding a number of 0.1 mm distance rings to raise the flange height. Appropriate spacers or extension rings are not provided with the lens mount. All FSMs delivered with this mount applied are adjusted accordingly to meet the correct back focal distance by C- and CS-Mount standard.

8.2 FMA-FC-150/60: Flex Cable for MIPI CSI-2 Connections

- FSA to FPA for MIPI CSI-2 connections (mandatory)
- Extension through “daisy-chaining” possible (maximum length is sensor and setup depending)
- Rigit-flex design (connectors on rigit PCBs)

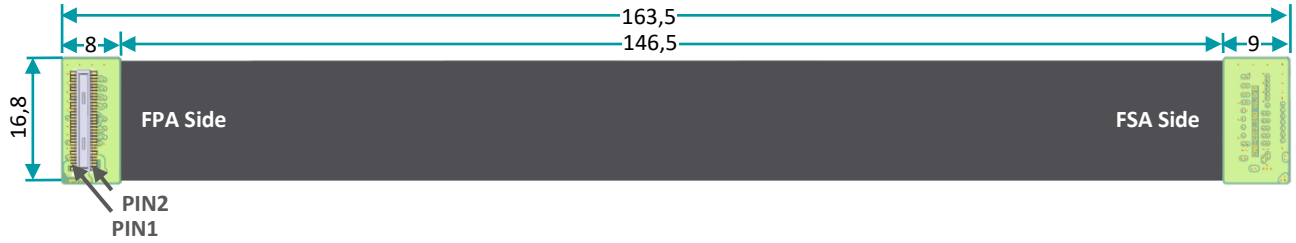
Note: Don’t use for any other connections than for MIPI CSI-2. Might lead to signal degrations and even damage!

8.2.1 Flex Cable Connectors

- FSA Side: Hirose DF40C-60DS-0.4V
- FPA Side: Hirose DF40C-60DP-0.4V
- Pin Assignment: Pin 1 to Pin 1

8.2.2 Mechanical Drawing and Pinout

Top Side



Bottom Side

8.3 FMA-FC-150/60-LVDS: Flex Cable for Sub-LVDS, SLVS and SLVS-EC Connections

- FSA to FPA for Sub-LVDS, SLVS and SLVS-EC connections (mandatory)
- Extension through “daisy-chaining” possible (maximum length is sensor and setup depending)
- Rigit-flex design (connectors on rigit PCBs)

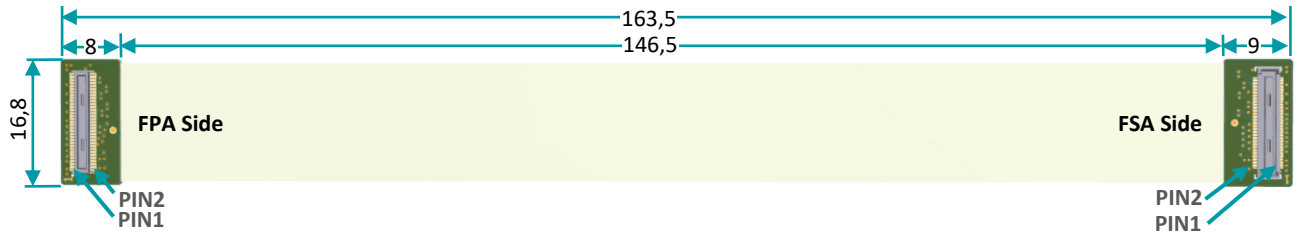
Note: Don’t use for MIPI CSI-2 connections. Might lead to signal degrations and even damage!

8.3.1 Flex Cable Connectors

- FSA Side: Hirose DF40C-60DS-0.4V
- FPA Side: Hirose DF40C-60DP-0.4V
- Pin Assignment: Pin 1 to Pin 1

8.3.2 Mechanical Drawing and Pinout

Top Side



Bottom Side

9 Software Package and Drivers

As FRAMOS we know that the getting started with a new technology is the biggest challenge. The idea behind the Software Package is to enable embedded software engineers to get quickly to a streaming system and provide at the same time all tools that are needed to extend and adapt it according the individual needs of the application.

What the software package and driver are:

- A reference for a custom sensor implementation
- Demonstrating how to use the required interfaces
- Demonstrating how to communicate with the image sensor
- Demonstrating how to generaly initialize and configure the image sensor
- Provide initial image streaming output to the user space
- Demonstrating how to run basic image processing on pixel data

What it is not:

- A fully featured camera implementation - not all sensors features might be implemented
- Ready to be use in the field
- A benchmark for the capabilities of the image sensor
- Focused on image processing

Supported Processor Platforms

The table below shows which platforms are supported by the standard driver package, and how many FSMs can at maximum be operated in parallel.

Sensor Module	NVIDIA Jetson TX2	NVIDIA AGX Xavier	NVIDIA Jetson Nano, Xavier NX	DragonBoard 410c	96Boards Consumer Edition	Xilinx Development Boards
FSM-AR0144	4		2		HW only, driver development on project basis.	
FSM-AR0521	4		2	2		
FSM-AR1335	4		2			
FSM-HDP230	4	4	2			
FSM-IMX264	2	4	-			
FSM-IMX283	2	4	-			
FSM-IMX290	4		2	2		
FSM-IMX296	4		2	2		
FSM-IMX297	4		2			
FSM-IMX304	2	4	-			
FSM-IMX327	4		2	2		
FSM-IMX334	2	4	-			
FSM-IMX335	4		2			
FSM-IMX412	4		2	2		
FSM-IMX415	4		2			
FSM-IMX462	4		2			
FSM-IMX464	4		2			
FSM-IMX477	4		2			
FSM-IMX485	4		2			
FSM-IMX577	4		2			
FSM-IMX530	2	4	-			1[3]

Table 22: Ecosystem Software Package - Supported number of FSMs per processing board

[3] SLVS-EC based FPGA reference implementation as part of the SLVS-EC RX IP Core offering.

9.1 Reference Software: NVIDIA Jetson Family

The software package provided with the Development Kits of the FRAMOS Sensor Module Ecosystem provided for NVIDIA Jetson platforms provides a reference implementation of sensor and device drivers for MIPI CSI-2. It contains a minimum feature set demonstrating how to utilize the platform specific data interface and communication implementation, as well as the initialization of the image sensor and implementation of basic features.

Package Content:

- Platform and device drivers with Linux for Tegra Support
- V4L2 based subdevice drivers (low-level C API)
- Streamlined V4L2 library (LibSV) providing generic C/C++ API
- Image Pre-Processing Examples:
    - OpenCV (Software)
    - LibArgus (Hardware)

Supported Devices:

- Jetson Nano (B01)
- Jetson TX2
- Jetson Xavier NX
- Jetson AGX Xavier

9.1.1 Platform and Sensor Device Drivers

The driver divides into two main parts that are configured in separate ways – the Image Modes and the General Features of the image sensor.

Image Modes

These are major attributes that have impact to the image data stream formatting. They require a static pre-configuration within the device tree (DT):

- Image / streaming resolution
- Pixel format / bit depth
- Data rate / lane configuration

Each driver provides access to 3 – 5 pre-built configurations, reflecting the main operation modes of the imager. Beside the full resolution, that is always available, they allow to receive image streams in common video resolutions like VGA, Full HD and UHD as they are supported or make sense by the imagers, and utilize sensor features like ROI and binning.

They act as an example for implementation and usage and are available as source. Due to the size limitation of the device tree, it is not possible to integrate an extensive set of options.

General Features

These are attributes of the image sensor that do not manipulate the data stream formatting. The drivers provided with the Software Pack integrate the sensor features as shown in the table below.

Pre-Implemented Features per Model	Gain (Analog / Digital)	Frame Rate	Exposure Time	Flip / Mirror	IS Mode (Master / Slave)	Sensor Mode ID	Test Pattern Output	Black Level	HDR Output	Broadcast	Data Rate	Synchronizing Master
FSM-AR0144												
FSM-AR0521												
FSM-AR1335												
FSM-HDP230												
FSM-IMX264												
FSM-IMX283												
FSM-IMX290												
FSM-IMX296		*										
FSM-IMX297		*										
FSM-IMX304												
FSM-IMX327												
FSM-IMX334												
FSM-IMX335												
FSM-IMX412												
FSM-IMX415												
FSM-IMX462												
FSM-IMX464												
FSM-IMX477												
FSM-IMX485												
FSM-IMX530												
FSM-IMX577												

V4L (libsv) and libargus
V4L (libsv)
Not Implemented

*Only supported in all pixel mode

Table 23: Supported sensor features on NVIDIA Jetson TX2 / AGX Xavier

Further features, as been supported by the image sensor, can be integrated into the driver sources using the image sensor datasheet.

9.1.2 Image Pre-Processing Examples

The provided image processing examples show the general mechanisms of data handling, for an image processing using 3rd-party IP. Both, the OpenCV and the LibArgus examples do not output data that is tuned for best visual experience.

LibArgus Example:

- Closed source ISP implementation
- Using hard ISP in NVIDIA Jetson SOCs
- Most performant option
- Example Implementation: Full but not tuned image pipeline, displaying

Color tuning and lens correction needs to be calibrated for every image sensor separately and depends on sensor and lens attributes as well as illumination situation.

Image Pre-Processing Features per Model	Bad Pixel Correction	Noise Reduction	Black Level Comp.	Auto Exposure, Gain	Auto White Balance	Demosaic	Color Correction	Color Artifact Suppr.	Downscaling	Edge Enhancement
FSM-AR0144										
FSM-AR0521										
FSM-AR1335										
FSM-HDP230										
FSM-IMX264										
FSM-IMX283										
FSM-IMX290										
FSM-IMX296										
FSM-IMX297										
FSM-IMX304										
FSM-IMX327										
FSM-IMX334										
FSM-IMX335										
FSM-IMX412										
FSM-IMX415										
FSM-IMX462										
FSM-IMX464										
FSM-IMX477										
FSM-IMX485										
FSM-IMX530										
FSM-IMX577										

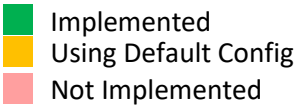


Table 24: Implemented LibArgus features for NVIDIA Jetson TX2 / AGX Xavier

Default Config

Image streaming is performed through the LibArgus pipeline, using a common configuration. It demonstrates the usage of LibArgus but is not optimized for the certain sensor configuration and might not lead to good image representation.

As NVIDIA camera partner, FRAMOS provides appropriate ISP tuning services on project basis for the individual customer system.

OpenCV Example:

- Open software library
- Easy to use and large feature set
- Extremely performance hungry (CPU)
- Not recommended for pre-processing
- Example Implementation: Demosaicing, Displaying

Image Pre-Processing Features per Model	Bad Pixel Correction	Noise Reduction	Black Level Comp.	Auto Exposure, Gain	Auto White Balance	Demosaic	Color Correction	Color Artifact Suppr.	Downscaling	Edge Enhancement
FSM-AR0144										
FSM-AR0521										
FSM-AR1335										
FSM-HDP230										
FSM-IMX264										
FSM-IMX283										
FSM-IMX290										
FSM-IMX296										
FSM-IMX297										
FSM-IMX304										
FSM-IMX327										
FSM-IMX334										
FSM-IMX335										
FSM-IMX412										
FSM-IMX415										
FSM-IMX462										
FSM-IMX464										
FSM-IMX477										
FSM-IMX485										
FSM-IMX530										
FSM-IMX577										

Implemented
Not Implemented

Table 25: Implemented features in OpenCV example

Due to limited performance and extreme resource utilization, it is not planned to enhance the image processing support on software side.

10 Ecosystem Compatibility Matrix

10.1 Hardware Support

The following matrix shows the compatibility of FSMs, FSAs and FPAs to each other. The FSAs differentiate to each other by supplied voltages, power up sequence, generated clock (oscillator) and physical attributes.

Sensor Modules with MIPI CSI-2 (D-PHY) Output

Item	FSM-IMX412 FSM-IMX477 FSM-IMX577	FSM-IMX290 FSM-IMX327 FSM-IMX334 FSM-IMX335 FSM-IMX462 FSM-IMX464 FSM-IMX485	FSM-IMX296 FSM-IMX297	FSM-AR0521 FSM-AR1335	FSM-IMX415	FSM-IMX283	FSM-AR0144	FSM-HDP230
FSA-FT1/A	FPA-4.A/TXA FPA-A/NVN FPA-2.A/96B FPA-ABC/XX1[4]							
FSA-FT3/A		FPA-4.A/TXA FPA-A/NVN[5] FPA-2.A/96B FPA-ABC/XX1[4]						
FSA-FT6/A			FPA-4.A/TXA FPA-A/NVN FPA-2.A/96B FPA-ABC/XX1[4]					
FSA-FT7/A				FPA-4.A/TXA FPA-A/NVN FPA-2.A/96B FPA-ABC/XX1[4]				
FSA-FT11/A					FPA-4.A/TXA FPA-A/NVN FPA-2.A/96B FPA-ABC/XX1[4]			
FSA-FT12/A						FPA-4.A/TXA FPA-2.A/96B FPA-ABC/XX1[4]		
FSA-FT13/A							FPA-4.A/TXA FPA-A/NVN FPA-2.A/96B FPA-ABC/XX1[4]	
FSA-FT19/A								FPA-4.A/TXA FPA-A/NVN FPA-2.A/96B FPA-ABC/XX1[4]

Table 26: Ecosystem Compatibility Matrix – Native CSI-2 (D-PHY) FSMs

[4] Not verified, Xilinx Development Board with hard MIPI CSI-2 / D-PHY interface.
[5] FSM-IMX334 is not supported due to the sensor requiring 4-lanes MIPI.

Sensor Modules with (Sub-) LVDS and SLVS Output

Item	Data Output (FSA)	FSM-IMX264	FSM-IMX304	FSM-IMX421	FSM-IMX530
FSA-FT14/A-00G	MIPI CSI-2	FPA-4.A/TXA FPA-2.A/96B FPA-ABC/XX1[4]			
FSA-FT15/A-00G	MIPI CSI-2		FPA-4.A/TXA FPA-2.A/96B FPA-ABC/XX1[4]		
FSA-FT18/A-00G	MIPI CSI-2				FPA-4.A/TXA FPA-2.A/96B FPA-ABC/XX1[4]
FSA-FT18/BC	SLVS, SLVS-EC				FPA-ABC/XX1
FSA-FT20/BC	SLVS, SLVS-EC			FPA-ABC/XX1	

Table 27: Ecosystem Compatibility Matrix – Sub-LVDS, SLVS and SLVS-EC FSMs